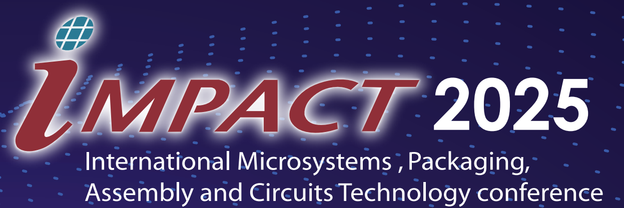

Final Program

Oct. 21-24 TaiNEX, Taipei, Taiwan

Energy-Efficient AI: From Cloud to Edge

IMPACT Official Site

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Tuesday October 21

Room	Grand Hilai Taipei 3F, Platinum Grand Ballroom B				
9:30-9:40	Opening & Award Ceremony				
9:40-10:30	<Plenary Speech I> Enabling energy-efficient AI with Semiconductor Innovations. Frank J.C. Lee, Ph.D, VP, TSMC				
10:30-11:20	<Plenary Speech II> Future Packaging/System Challenges for AI Data Centers. Babak Sabi, Ph.D, VP, AWS				
11:20-12:10	<Plenary Speech III> Architecting the Future: Innovations in Scalable Data Center Design. Jatin Upadhyay, VP, Intel				
12:10-13:00	Lunch Break/ back to TaiNEX I				
Room	504 a	504 b	504 c	503	502
13:00-15:00	【 S1 】 Strategic Breakthroughs in High-Density Server Design: Elevating Compatibility and Performance (Intel)	【 S2 】 Enabling AI and HPC: Technology Inflections Across Advanced Packaging and Interconnect (MKS 'Atotech)	【 S3 】 Component to System-Level Integration (GEA)	【 S4 】 Cu-Cu & Hybrid Bonding	【 S5 】 Advanced Characterization & Materials Behavior in Electronic Packaging
15:00-15:30	Poster session I (Packaging)				
15:30-17:45	【 S6 】 AMD Server Solution Customer SI+EV Enablement (AMD)	【 S7 】 AI Packaging Supply Chain Ecosystem & Driving Technology (Applied Materials)	【 S8 】 Thermal-Mechanical Modeling & Simulation I	【 S9 】 Interconnections & Nanotechnology	【 S10 】 Metallization & Advanced Substrate Process Integration
18:00-20:30	IMPACT 20th Anniversary Welcome Dinner (Invited Only)				

Wednesday October 22

Room	504					
9:00-9:50	<Plenary Speech IV >The need for chiplet - based SoC technologies in the automotive industry. Takao Iwaki, Ph.D, Director, MIRISE Technologies					
Room	504 a	504 b	504 c	503	502	501
10:10-12:10	【 S11 】 Advanced Packaging and Metrology Technologies (ICEP)	【 S12 】 Fusion Interconnect of Electrical and Optic for Energy Efficiency (ASE)	【 S13 】 Heterogeneous Integration	【 S14 】 Thermal-mechanical Modeling & Simulation II	【 S15 】 Power Electronics	【 S16 】 Bonding, Dielectric Materials, and Laser-Material Interactions
12:10-13:00	Lunch Break					

Room	504 a	504 b	504 c	503	502
13:00-15:00	【 S17 】 Redefining Advanced Packaging with Glass Core Solution (Hi-CHIP)	【 S18 】 Enhanced Energy Efficiency in AI: Advanced Packaging and PCB Technologies for Sustainable Innovation (Qnity™, DuPont Electronics)	【 S19 】 Deep Learning for Geometry & Mechanics Prediction	【 S20 】 Advanced Materials, Automatic Process & Assembly	【 S21 】 Materials and Interfaces for Reliable Electronics
15:00-15:30	Poster session II(Packaging+PCB)				

Room	504 a	504 b	504 c	503	502	501
15:30-18:00	【 S22 】 Reliaiblity and Thermal Management of Advanced Packages (ISMP)	【 S23 】 IEEE EPS: Materials and Technologies for Advanced Packaging (SPIL)	【 S24 】 Process & Manufacturing in Advanced packaging	【 S25 】 Characterization, Testing, & Inspection in Advanced Packaging	【 S26 】 Thermal characterization & Management	【 S27 】 Smart Manufacturing and System Modeling

Thursday October 23

Room	504			
9:00-9:50	<Plenary Speech V> Reimagining Advanced Packaging with Glass: Opportunities and Challenges. Sung Jin Kim, Ph.D, CTO, Absolics			
Room	504 b	504 c	503	502
10:10-12:10	【 S28 】 Convergence or Divergence? Panel-Level Packaging Meets Heterogeneous Integration (Lam Research)	【 S29 】 Manufacturing Processes in Advanced Packaging	【 S30 】 Electrical Characterization & Simulation	【 S31 】 Interconnect & Interface Technologies for Advanced Electronic Systems
12:10-13:00	Lunch Break			

Room	504 a	504 b	504 c	503	502	4F L-1308
13:00-15:00	【 S32 】 Glass Packaging	【 S33 】 3D Embedding	【 S34 】 Materials & Processes for Advanced Packaging from Japan (JIEP)	【 S35 】 Scalable Modeling in Advanced Packaging	【 S36 】 Advanced Materials & Processing for Electronic Packaging	【 S37 】 AI-Powered in Semiconductor Packaging (TPCA)

Room	504 c	502	4F L-1308
15:10-18:10	PDC1Kuan-Neng Chen: 3D IC and Advanced Packaging: Fundamentals, Hybrid Bonding, Innovations and Future Perspectives	PDC2 Andrew Tay: Analysis of Fracture and Delamination in Microelectronic Packages	【 S38 】 15:10~17:00 AI HW Process and Metrology : Soldering, Package, TGV and PCB (SMTA Taiwan Chapter)

Plenary Speech	PCB Session
Industrial Session	Open Seminar
Special Session	Poster
Packaging Session	PDC

*The organizer reserves the right to modify the agenda.

Floor Plan

IMPACT 2025

Conference Room

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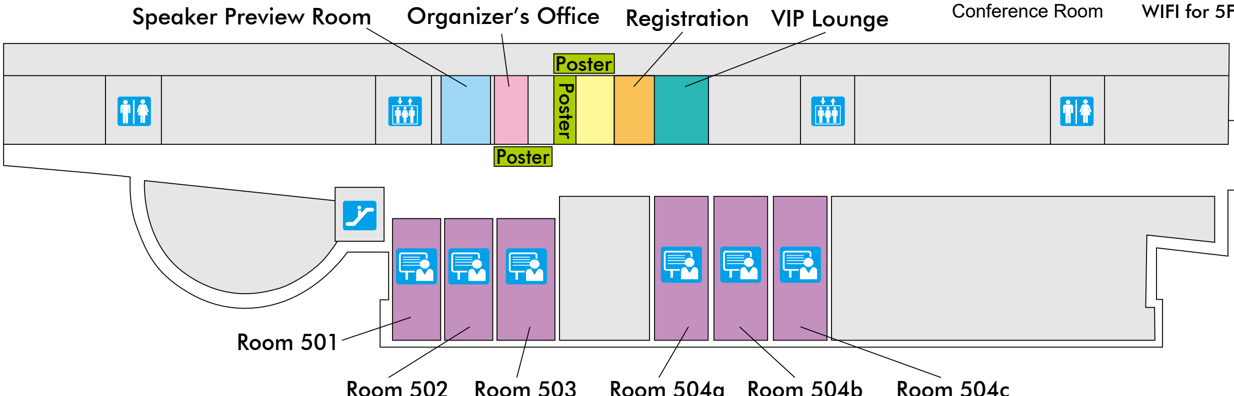
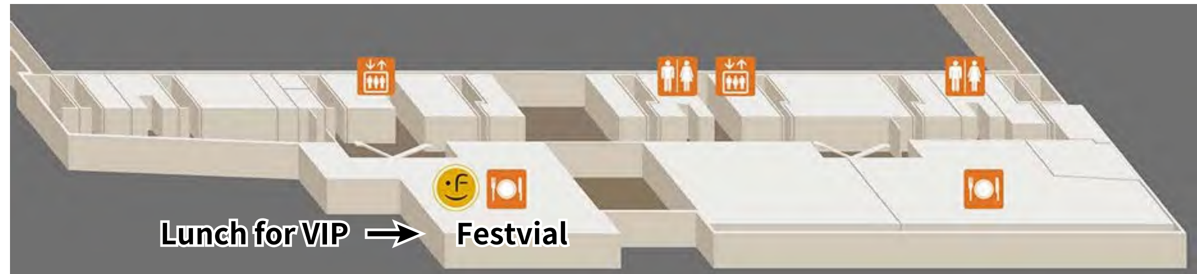
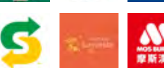


TPCA Show
TAIPEI





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Organizer

IEEE ELECTRONICS PACKAGIMG SOCIETY

台灣國際微電子暨構裝學會

INTERNATIONAL MICROELECTRONICS AND PACKAING SOCIETY TAIWAN (IMAPS Taiwan)

INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE, TAIWAN (ITRI)

TAIWAN PRINTED CIRCUIT ASSOCIATION (TPCA)

Co-Organizer

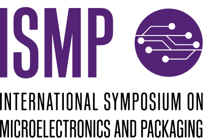
Feng Chia University(FCU)

Graduate Institute of Communication Engineering

Global Electronics Association

International Conference on Electronics Packaging (ICEP)

International Electronics Manufacturing Initiative (iNEMI)



International Symposium on Microelectronics and Packaging(ISMP)

I-Shou University (ISU)

The Japan Institute of Electronics Packaging(JIEP)

National Tsing Hua University (NTHU)

Surface Mount Technology Association (SMTA)

Taiwan Semiconductor Industry Association (TSIA)

Taiwan Thermal Management Association (TTMA)

Industrial Session

Advanced Micro Devices, Inc. (AMD)

Applied Materials, Inc.

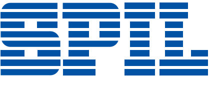
Advanced Semiconductor Engineering, Inc. (ASE)

Qnity™, DuPont Electronics

Intel

Lam Research

MKS' Atotech

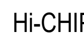


Siliconware Precision Industries Co., Ltd (SPIL)

Supporter

C SUN MFG. LTD.

Eternal Materials Co.,Ltd.


Hi-CHIP

Ichia Technologies., INC.

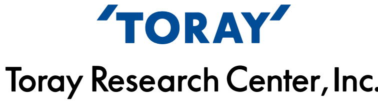
JCU CORPORATION

JSR Corporation

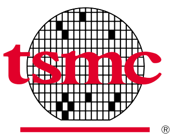
MacDermid Performance Solutions Taiwan Ltd.

OKUNO CHEMICAL INDUSTRIES CO., LTD.

Omron Corporation



Toray Research Center, Inc.



Taiwan Semiconductor Manufacturing Company Limited (TSMC)

United Microelectronics Corporation (UMC)

Unimicron Technology Corporation

Universal Scientific Industrial Co., Ltd (USI)

Partner

EPTC

TechSearch International

YOLE Group

Goverment Sponsor

Ministry of Education

National Science and Technology Council

Welcome Message from Shih-Chieh Chang, Conference General Chair

Shih-Chieh Chang, Ph.D.
General Chair of IMPACT 2025
Vice President & General Director
Electronic and Optoelectronic System Research Laboratory
Industrial Technology Research Institute

Dear Experts, Colleagues and Friends,

It is my great pleasure, on behalf of the IMPACT 2025 committee, to warmly welcome all participants to this year's conference, held from October 21 to 24, 2025, at the Taipei Nangang Exhibition Center.

With the theme "Energy-Efficient AI – From Cloud to Edge," IMPACT 2025 will highlight how advanced packaging and system integration technologies enable artificial intelligence to achieve new levels of efficiency, performance, and sustainability. This year's program features five plenary talks, an EPS panel, 16 special forums (including 10 industry-sponsored), and over 200 oral and poster presentations, with contributions from more than 300 experts and researchers worldwide.

For 20 years, ITRI and IMPACT have partnered to advance packaging and system integration, contributing significantly to the semiconductor field. As IMPACT celebrates its 20th anniversary, we have prepared activities such as AI photo Interaction, the Legacy Explorer challenge, limited-edition gift cards, and more, which honor two decades of achievement and strengthen connections among participants. We look forward to continuing this partnership and creating new milestones together.

I sincerely thank our Technical Program Committee and partner organizations—IEEE EPS-Taipei, iMAPS-Taiwan, ITRI, and TPCA—for their dedication in shaping such a rich and diverse program.

We also invite you to explore the vibrancy of Taipei—its culture, cuisine, and hospitality. May your time here be both professionally rewarding and personally memorable.

Thank you once again for joining IMPACT 2025. I wish you an inspiring and successful conference.

Sincerely,

Shih Chieh Chang

Shih-Chieh Chang, Ph.D.
General Chair of IMPACT 2025
Vice President & General Director
Electronic and Optoelectronic System Research Laboratory
Industrial Technology Research Institute

Welcome Message from K. N. Chiang, Conference Honorary Chair

K. N. Chiang, Ph.D.
Chair Professor, National Tsing Hua University
Academician, International Academy of Engineering (IAE)
Fellow, IEEE / STAM / ASME / iMAPS / AIIA / AIAA
Distinguished Research Fellow, National Science and Technology Council

It is my honor to welcome you all to IMPACT 2025 in Taipei! This special event brings together colleagues from across the globe to share, learn, and inspire one another in the exciting fields of AI/ Machine learning, simulation, advenced packaging, and PCBs. IMPACT annually attracts more than 600 participants, features over 200 papers.

This year's program is designed to highlight emerging technologies and key industry trends, with sessions covering power module packaging, Chiplets, heterogeneous packaging, 3D/system-in-package (SiP), fan-out packaging, automotive applications, high-performance computing, AI and machine learning, as well as advanced design-on-simulation technologies.

I sincerely hope you find the sessions engaging, the discussions inspiring, and the networking fruitful. Thank you for joining us, and I wish you every success during this important gathering.

K. N. Chiang, Ph.D.
Chair Professor, National Tsing Hua University
Academician, International Academy of Engineering (IAE)
Fellow, IEEE / STAM / ASME / iMAPS / AIIA / AIAA
Distinguished Research Fellow, National Science and Technology Council

Welcome Message from Shin-Puu Jeng, Conference Co-Chair

Shin-Puu Jeng, Ph.D.
Co-Chair of IMPACT 2025
President, IMAPS-Taiwan

Dear Colleagues and Friends,

It is a great pleasure to welcome you to the 2025 IMPACT Conference—the 20th International Microsystems, Packaging, Assembly, and Circuits Technology Conference. This year's theme, Energy-Efficient AI: From Cloud to Edge, highlights a defining challenge of our time: delivering ever-greater computing power while managing energy consumption responsibly.

The technologies enabling this transformation are evolving at unprecedented speed. Heterogeneous integration and co-packaged optics are reshaping advanced packaging, creating high-bandwidth, low-power interconnects. At the same time, progress in silicon devices, PCB technologies, and system architectures is driving efficiency gains across every layer of computation. Crucially, sustainable AI innovation must extend beyond cloud data centers to the edge, where localized, energy-aware processing reduces reliance on centralized infrastructure. By empowering the edge, we can cut latency, save bandwidth, and lower overall system power.

Such advances can only succeed when pursued collectively. From materials to systems, from design to deployment, progress in energy-efficient AI depends on cross-disciplinary expertise and collaboration. This is the essence of IMPACT: uniting leaders from industry, academia, and research to exchange insights, tackle challenges, and shape new directions.

Thank you for joining us at IMPACT 2025. I look forward to the ideas, discoveries, and partnerships that will emerge as we work together to build a future where AI is both powerful and energy-conscious—from the cloud to the edge.

Best Wishes,

Shin-Puu Jeng

Shin-Puu Jeng, Ph.D
Co-Chair of IMPACT 2025
President, IMAPS-Taiwan

Welcome Message from C. Robert Kao, Conference Co-Chair

C. Robert Kao, Ph.D.
Chair, IEEE EPS – Taipei
Distinguished Professor, National Taiwan University

Imagine an AI ecosystem that learns faster while consuming far less energy—welcome to IMPACT 2025, where innovators converge to bridge cloud-scale intelligence and edge-deployed efficiency.

On behalf of the IMPACT 2025 Organizing Committee, it is my great pleasure and honor as Co-Chair to formally welcome you to the 2025 International Microsystems, Packaging, Assembly and Circuit Technology Conference (IMPACT 2025).

IMPACT 2025, organized by IEEE-EPS Taipei, iMAPS-Taiwan Chapter, ITRI, and TPCA, is the premier gathering of PCB, packaging, and system-integration professionals in Taiwan. This year's event will take place October 21–24, 2025, at the Taipei Nangang Exhibition Center, in conjunction with TPCA Show 2025. Under the theme "Energy efficient AI – From Cloud to Edge," we will explore low-power AI hardware, edge-computing architectures, data-center optimizations, and sustainable design strategies, fostering collaboration across industry and research communities.

We are proud to collaborate with leading international organizations—ICEP and JIEP from Japan, iNEMI and IEEE EPS from the USA—and global consultancies such as Yole Développement and TechSearch. Their insights will enrich our plenary sessions, technical tracks, and networking events, offering a comprehensive view of the energy-efficient AI ecosystem.

Join us at IMPACT 2025 to engage with cutting-edge technologies, connect with global experts, and help shape the future of intelligent systems from cloud to edge. Your participation will drive innovation and advance sustainable solutions in electronic packaging and integration.

Best regards,

C. R. Kao

C. Robert Kao, Ph.D.
Co-Chair of IMPACT 2025
Distinguished Professor, National Taiwan University

Welcome Message from Yu Hua Chen, Conference Co-Chair

Yu Hua Chen, Ph.D.
Co-Chair of IMPACT 2025
Convenor of Semiconductor Packaging Committee, TPCA
Vice President, Unimicron Technology Corp.

Distinguished guests, industry leaders, technology partners, and all participants of the IMPACT Conference: Welcome!

It's my pleasure to welcome you all to the 20th IMPACT Conference on behalf of the Conference Co-Chair. This year, our theme is "Energy Efficient AI – From Cloud to Edge," exploring how, amidst the rapid evolution of AI technology, innovative packaging and system integration can achieve more efficient and sustainable computing architectures. Since its inception, the IMPACT Conference has witnessed the evolution of packaging technology from traditional to advanced, and from single chip to heterogeneous integration. Today, we not only celebrate this history, but also look to the future, focusing on the new challenges and opportunities brought by AI applications—from cloud data centers to edge devices, energy efficiency has become a key metric for technological development. This conference brings together experts and industry leaders from around the world delving into cutting-edge technologies such as chip packaging, thermal management, system integration, and low-power design. We believe that cross-disciplinary exchange and collaboration will inspire more innovative ideas and promote the sustainable development of AI technology and the semiconductor industry. I would like to express my sincere gratitude to all of you for your attendance and support, and to all the speakers and the organizing team for their meticulous preparation. We wish this conference will be a great success, and hope that everyone will gain valuable insights and knowledge from IMPACT Conference.

Best Regards,

Yu-Hua Chen, Ph.D.
Co-Chair of IMPACT 2025
Convenor of Semiconductor Packaging Committee, TPCA
Vice President, Unimicron Technology Corp.

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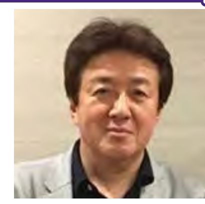

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Promotion & Public Relations
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General Information of IMPACT 2025

Since its inception in 2006, the IMPACT Conference has been at the forefront of technological evolution, fostering innovation in the packaging, PCB, and semiconductor industries. Over the past two decades, IMPACT has not only witnessed but actively contributed to rapid advancements in 5G, AI, high-performance computing (HPC), edge computing, and sustainability. Each year, the conference has adapted to the latest trends, driving forward the conversation on emerging technologies and their industrial applications.

Now in its 20th year, IMPACT 2025 embraces the theme "Energy-Efficient AI: From Cloud to Edge" reflecting the industry's growing emphasis on high-performance, low-power solutions. As AI applications continue to expand—from data centers to edge devices—the need for advanced PCB, IC substrates, heterogeneous integration, and packaging technologies has become increasingly critical.

This milestone year marks not just a celebration of the past 20 years, but a bold step into the future, where IMPACT continues to lead, inspire, and drive innovation. Join us at IMPACT 2025 as we shape the next era of AI, semiconductor packaging, and PCB technology—powering a smarter, more sustainable world.

About Conference

- **Date:** October 21(Tue) – October 24 (Fri), 2025
- **Opening Venue:** Grand HiLai Taipei 3F
- **Main Venue:** 5F Taipei Nangang Exhibition Center, Hall 1, Taipei (TaiNEX 1)
- **Exhibition:** TPCA Show、TAITRONICS
- **Theme:** Energy-Efficient AI: From Cloud to Edge

Registration Desk

Please check in and get badge & conference materials as following times

Opening ceremony

10/21 8:30-11:20 3F, Grand Hilai Taipei

Main Registration

10/21 11:00-16:30 5F, TaiNEX 1

10/22 08:30-16:30 5F, TaiNEX 1

10/23 08:30-16:30 5F, TaiNEX 1

Organizer Office & Speaker Preview Room

For ORAL presenter, please do arrive at the Preview Room 1 hour before your presentation to store your ppt files if any update.

Location: 5F, TaiNEX 1

Open Hour:

10/21 10:00-17:00

10/22 08:00-17:00

10/23 08:00-17:00

Poster Session (Interactive Session)

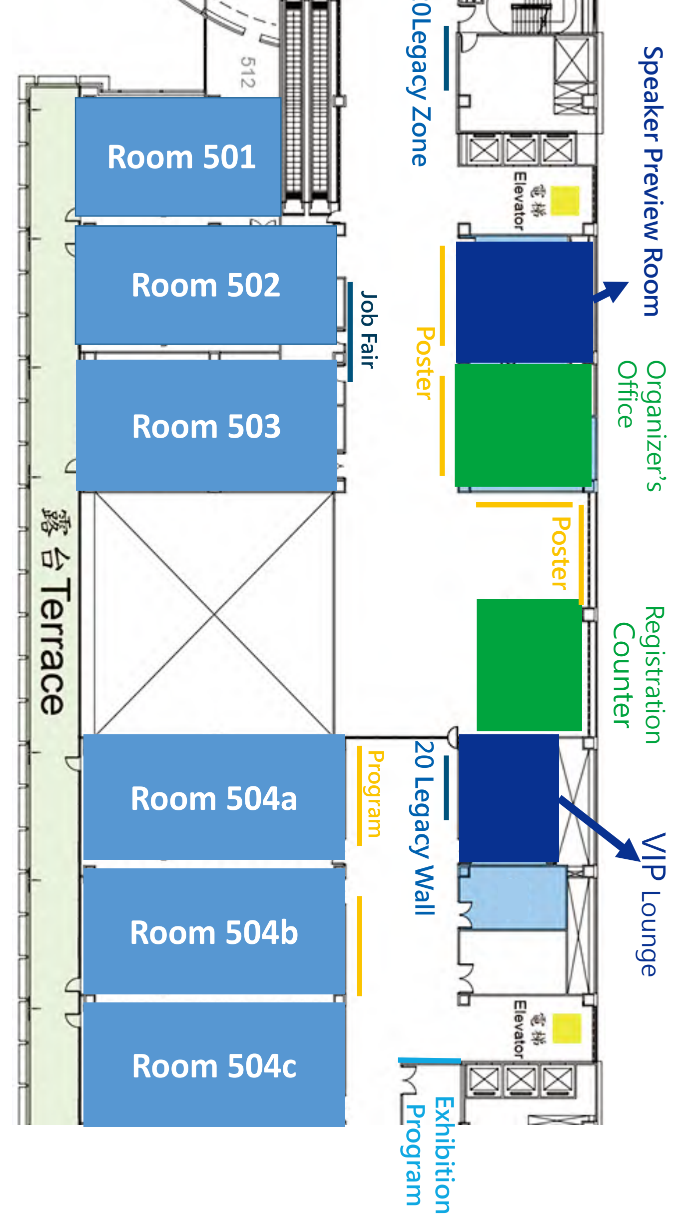
For POSTER presenter, please display & stand by your poster during your presentation time

Location: Foryer Area, 5F, TaiNEX 1

Date/Time:

Poster Session I –15:00-15:30 pm, Oct. 21, 2025

Poster Session II –15:00-15:30 pm, Oct. 22, 2025



Lunch for VIP

Date/Time: 11:30-13:30, Oct. 21-23, 2025
Location: Festival Restaurant at 3rd floor TaiNEX 1

Access: VIPs with lunch tickets (including Plenary Speakers, Invited Speakers, Session Chair, and Committee Members)
You could also find dining places on 1st Floor or nearby buildings

Welcome Dinner (By invitation only)

Time: Oct. 21, 2025 (18:00 – 20:30)
Venue: 3F Ballroom, Grand Hi-Lai Hotel, Taipei
(台北漢來大飯店3樓宴會廳)
Address: NO. 168, JINGMAO 1ST RD., NANGANG DIST., TAIPEI CITY 115 , TAIWAN
(台北市南港區經貿一路168號)
TEL: (02) 2788-6868
Access: Open to invited guests (Plenary Speakers, Invited speakers, Sponsors, VIP, Committee members)

TPCA Show

Time: Oct. 22-24. 2025 (10:00 – 17:00) *24 Oct till 15:00
Venue: 1F & 4F, TaiNEX1

Internet Access

Wireless internet is provided on 5th floor of Taipei Nangang Exhibition Center for free.

Identification of Badges

Badges are required for admittance to all sessions and access to TPCA Show. Please bring it with you all the time.

Conference Venue

Conference rooms will be located on the 5th floor of Taipei Nangang Exhibition Center.

TWTC Nangang Exhibition Hall Transport & Parking Information

Neihu · Donghu
Keelung River
Nanhu Bridge
Huandong Blvd
Park
Business
Nangang
MRT Nangang Software Park Station
NKSP Ⅰ、Ⅱ
NKSP Ⅲ
TWTC Nangang
TWTC Nangang 2 (under construction)
MRT TWTC Nangang Station
Nangang Vocational High School
Cheng-Zheng Junior High School
North-south railway(Western Line)
Nangang Connecting Highway
Sijhih
Nangang

Parking Lots：

- P1 TWTC Nangang／620 Parking spaces
- P2 Taiwan Fertilizer C2 Parking Lot／352 Parking spaces
- P3 Taiwan Fertilizer C3 Parking Lot／768 Parking spaces
- P4 Taiwan Fertilizer C4 Parking Lot／82 Parking spaces
- P5 MRT Neihu Depot Parking Lot／584 Parking spaces／During Exhibition Periods
- P6 Xingzhong Parking Tower／647 Parking spaces／NT$30(per hour)／24HR

P Underground Parking
P Parking Lot
Entrance / Exit
Directions to TWTC Nangang

The parking fee above is for reference only

Transport Information：

1. Shuttle Bus Stop (Pick-up / Drop-off)
2. Bus Stop
3. Taxi Drop-off
4. Small Vehicle Drop-off
5. B1 Taxi Pick-up
6. Underground Parking Entrance
7. MRT Shuttle Bus Stop (to MRT Nangang Station)

2010.05

Contact: Ms. Mickey Huang/ Tel: +886-3- 3815659#405 / Email:service@impact.org.tw

IMPACT Best Paper 2024

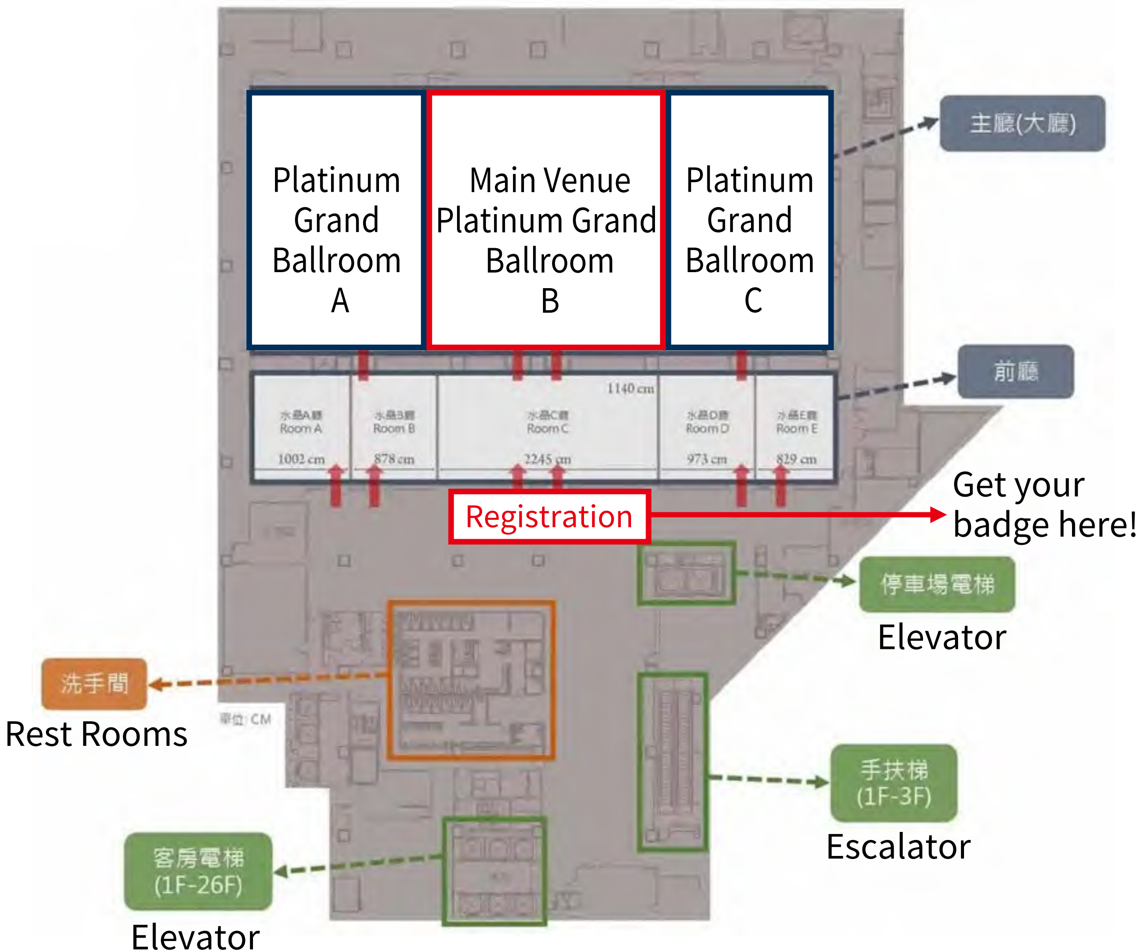
IMPACT 2024 received around 155 papers, and we have conducted the 3 stage paper review process including abstract, full paper, and onsite oral presentation. Thanks to the IMPACT Technical Program Committees, paper reviewers, and session chairs' great support, we are delighted to announce those papers that have been selected for the IMPACT 2024 Paper Award.

Award Category	Paper Code	Paper Title	Author List	Affiliation
Packaging - Best Paper Award	EU0181	Pioneering the leading-edge adhesion enhancement system for the future of package substrates bonding	Thomas Thomas, Christopher A. Seidemann, Thomas Huelsmann, Valentina Belova-Magri, Martin Thoms, Christian Noethlich, Fabian Michalik, Josef Gaida, Stefanie Ackermann, Yuan Zou, Andry Liong, Frank Bruening	Atotech Deutschland GmbH
	US0028	Predicting Wrinkle Formation in Flexible Thin-Film Structures	Yu-Lin Shen	University of New Mexico
	TW0010	Advanced Optical Metrology Using on Surface Morphology Characterization of Polyimide for Process Quality Enhancement	Kan-Ju Yang, Wen-Yi Lin, Chia-Peng Sun, Kai-Cheng Chen, Zhi-Hua Zou	Taiwan Semiconductor Manufacturing Company
Packaging -Best Student Award	TW0155	Power Efficiency Characterization of Bidirectional Bridgeless Interleaved Totem-Pole PFC Boost Converter Using SiC-Based Power Module	Wen-You Jhu, Hsien-Chie Cheng, Yu-Cheng Liu, Yan-Cheng Liu, Chun-Kai Liu, Tao-Chih Chang	Feng Chia University
	TW0167	Using Uncertainty Analysis to Validate Reliability Prediction in WLP with Idealized Solder Joint Modeling	Yu-Ting Su, Kuo-Ning Chiang	National Tsing Hua University
	TW0166	Developing Pad Design Criteria for Wafer-Level Chip-Scale Package Through Pad Size Effect Analysis	Chih-An Yang, Ying-Ju Chen, Kuo-Ning Chaing	National Tsing Hua University
Packaging-Best Poster Award	TW0017	Pre-fabricated Via Array Substrate for Programmable AIoT Applications	T. Y. Ouyang, Y. P. Chan, H. C. Fu, and H. H. Chang	ITRI
PCB-Best Paper Award	US0156	Productivity Enhancement in Semiconductor Manufacturing with AI-enabled Operations Digital Twin Platform	Amin Arbabian, Aria Pezeshk, Kaipei Yang	Plato Systems, Stanford University
	US0027	The Impact of Recent Revision of ENEPIG Specification - IPC 4556A	Frank Xu Ph.D, Martin Bunce	MacDermid Alpha Electronics Solutions
PCB-Best Student Award	TW0173	Inspection, Estimation, and Design of Hybrid Bonding in 3D IC Fabrication Using In-situ Heating Atomic Force Microscopy	Huai-En Lin, Wei-Lan Chiu, Hsiang-Hung Chang, Chih Chen	National Yang Ming Chiao Tung University
	TW0095	Optimization of High Aspect Ratio Through Glass Vias Void-Free Filling Using Complex System Response Platform	Yu-Ting Fu, Yiu-Hsiang Chang, Chih-Ming Ho, Da-Jeng Yao	National Tsing Hua University
PCB-Best Poster Award	TW0049	Advanced PCI Express Receiver Channel Signal Quality Validation For AI Server	Dian-Ying Wu, Denis Chen, Green Chen	Intel

Opening Ceremony

Time: 09:30-12:10, Tuesday, October 21, 2025
Location: Grand Hi-Lai Taipei 3F, Platinum Grand Ballroom B
Chair: Shih Chieh Chang, Ph.D., General Chair of IMPACT 2025
Please use your badge or QR code for access

Time	Agenda
09:28-09:30	Opening Video - 20 legacy
09:30-09:35	Welcome Remarks by Shih-Chieh Chang,General Chair of IMPACT 2025
09:35-09:40	IMPACT 2024 Best Paper Award Ceremony
09:40-10:30	<Plenary Speech I> Enabling energy-efficient AI with Semiconductor Innovations. Frank J.C. Lee, Ph.D, VP, TSMC
10:30-11:20	<Plenary Speech II> Future Packaging/System Challenges for AI Data Centers. Babak Sabi,Ph.D,VP of Technology, Annapurna Lab, AWS
11:20-12:10	<Plenary Speech III> Architecting the Future: Innovations in Scalable Data Center Design. Jatin Upadhyay, VP, Intel



PLENARY SPEECH

Tuesday, Oct. 21st, 09:40-10:30

Dr. Frank J. C. Lee

Vice President
Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC)

Topic: Enabling energy-efficient AI with Semiconductor Innovations

Room 3F,Grand HiLai Taipei

Abstract:

As artificial intelligence workloads scale exponentially, energy efficiency has emerged as a critical bottleneck in sustaining performance growth. This keynote explores how TSMC's advanced semiconductor technologies are reshaping the energy-performance landscape for AI. We will highlight the latest innovations across process nodes, 3D integration, and advanced packaging—including CoWoS®, InFO®, and the COUPE architecture—that are purpose-built to reduce energy per operation while supporting massive compute density. The talk will delve into how TSMC's technology platforms enable AI accelerators, GPUs, and edge AI chips to achieve unprecedented power efficiency, addressing both datacenter and edge deployment challenges. By bridging silicon scaling and system-level optimization, TSMC is empowering its ecosystem to build sustainable AI infrastructure for the future.

Bio:

Frank earned his Ph.D. from Carnegie Mellon University in Pittsburgh, Pennsylvania. He is currently a Vice President at TSMC Technology Inc. in San Jose, California, where he leads the Custom Design Methodology group. His work focuses on advancing analog/RF design automation and migration for cutting-edge nodes, as well as pioneering 3D COUPE silicon photonics design and analysis methodologies. Prior to his role at TSMC, Frank served as Vice President at Synopsys in Mountain View, California. During his tenure there, he significantly contributed to a diverse array of products, including IR/EM analysis, RC extraction, advanced delay calculation, static timing analysis, timing optimization, advanced placement and routing, physical synthesis, cell characterization, and both SPICE and fast SPICE circuit simulation.

Tuesday, Oct. 21st, 10:30-11:20

Dr. Babak Sabi

VP of Technology, Annapurna Lab
AWS

Topic: Future Packaging/System Challenges for AI Data Centers

Room 3F,Grand HiLai Taipei

Bio:

Dr. Babak Sabi is VP of Technology at AWS/Annapurna Lab. Babak joined AWS in 2024 after 40 years in Intel. Babak was Senior Vice President and the General Manager of Assembly & Test Technology Development (ATTD) at Intel Corporation. Since 2009, he has been responsible for the company's packaging, assembly, and test process technology development. During Babak's tenure in ATTD 2.5D and 3D Advanced Packages were developed and ramp to high Volume Manufacturing. Additionally ATTD team made many advancement in Substrate and Test Technology.

Prior to leading ATTD, Babak oversaw Intel's Corporate Quality Network from 2002 to 2009 where he led product reliability, customer satisfaction and quality business practices.

Babak joined Intel in 1984 after receiving Babak his Ph.D. in solid state electronics from Ohio State University in 1984.

Tuesday, Oct. 21st, 11:20-12:10

Jatin Upadhyay

Vice President, Systems Integration and Engineering, Data Center and AI
Intel

Topic: Architecting the Future: Innovations in Scalable Data Center Design

Room 3F,Grand HiLai Taipei

Abstract:

As data centers rapidly evolve to meet the increasing demands of AI and high-performance computing, architectural innovation is more critical than ever. This presentation addresses the complex challenges of modern data center design—from node-level integration to full-scale infrastructure orchestration. It highlights Intel's innovation pillars, including advancements in memory technologies, high-speed interconnects, power delivery, thermal management, and software-defined infrastructure. Through a co-design approach across hardware and software, Intel showcases scalable solutions that enhance performance, efficiency, and reliability. Real-world applications—from healthcare to agriculture—demonstrate the transformative impact of these technologies. The session underscores the importance of industry collaboration and open standards, inviting ecosystem partners to join Intel in shaping the future of data center and AI infrastructure.

Bio:

Jatin leads the Data Center (Xeon) Customer and Systems Engineering team within Intel's Platform Engineering Group. He is responsible for overseeing and driving all aspects of front-line customer engineering, including managing customer requirements, resolving customer issues, ensuring customer readiness and acceleration, enabling industry and ecosystem partnerships, and fostering joint technology innovations.

Jatin began his career at Intel in 1995 as a chipset validation engineer and has since led various validation activities, including Pre-Silicon Systems, functional validation, IO/electrical validation, power/performance, customer enabling, Circuit Marginality Validation, and tester debug.

With extensive experience across mobile, micro-server, cable modem, and data center segments, Jatin is passionate about developing the next generation of leaders, building high-performing organizations, and driving innovation and efficiencies. He holds a Master's degree in Computer Architecture and an MBA in Engineering Management, and has multiple publications in parallel processing.

Wednesday, Oct. 22nd, 09:00-09:50

Dr. Takao Iwaki
Director, SoC R&D Div.
MIRISE Technologies Corporation

Topic: The need for chiplet-based SoC technologies in the automotive industry

Room 504, TaiNEX 1

Abstract:

In advanced driver assistance systems and autonomous driving, sophisticated AI technologies are employed for functions such as object recognition, self-localization, and trajectory planning. Since the required AI performance varies depending on vehicle type, a wide range of SoCs (Systems on Chip) is needed—from a few TOPS to over 1,000 TOPS per generation. Developing each of these individually is impractical, which is why chiplet technology—where multiple chips are modularly combined like LEGO blocks—is attracting growing interest.

For automotive applications, key technical challenges include ensuring package reliability under harsh environmental conditions and maintaining stable, high-bandwidth communication between chiplets. Addressing these issues is essential for the successful deployment of chiplet-based SoCs in vehicles. This presentation will explore the challenges and potential solutions surrounding chiplet integration in the automotive domain.

Bio:

Takao Iwaki received his B.Sc. and M.Sc. degrees in Physics from the University of Tokyo, Japan, in 1995 and 1997, respectively, and a Ph.D. degree in Engineering from the University of Warwick, U.K., in 2008.

He has been with DENSO CORPORATION since 1997, where he has primarily engaged in the research and development of MEMS (Micro Electro Mechanical Systems)-based automotive sensors, working both in business units and research laboratories. Since 2020, he has been seconded to MIRISE Technologies Corporation, an automotive semiconductor R&D company jointly funded by Toyota and DENSO. At MIRISE, he has led the research and development of automotive SoCs (Systems on Chip), initially as Director of the Planning and Administration Division and currently as Director of the SoC R&D Division. In 2023, he began working concurrently with ASRA (Advanced SoC Research for Automotive), focusing on chiplet-based SoC technologies for automotive applications.

Thursday, Oct. 23rd, 09:00-09:50

Dr. Sung Jin Kim
CTO
Absolics Inc.

Topic: Reimagining Advanced Packaging with Glass: Opportunities and Challenges

Room 504, TaiNEX 1

Abstract:

The evolution of semiconductor packaging technologies demands materials that surpass the limitations of traditional organic and silicon-based substrates. Among emerging candidates, glass has gained momentum as a transformative platform for next-generation applications in artificial intelligence (AI), high-performance computing (HPC), and radio frequency (RF) communication.

Glass substrates offer a unique combination of properties—low dielectric loss, high insulation resistance, exceptional dimensional stability, and thermal compatibility with silicon—that enable superior electrical performance and mechanical reliability. Their ultra-smooth surfaces and ability to support fine-pitch interconnects and high-aspect-ratio Through-Glass Vias (TGVs) further enhance signal integrity and miniaturization potential.

Unlike organic materials, glass provides excellent hermeticity and environmental resistance, making it ideal for advanced MEMS and optical packaging. Moreover, large-panel glass processing offers a scalable and cost-efficient path for high-volume manufacturing, extending benefits beyond performance to production economics.

However, widespread adoption faces challenges such as mechanical fragility, TGV metallization reliability, limited thermal conductivity, and the need for ecosystem readiness. Addressing these hurdles through material innovation, process optimization, and industry collaboration is critical.

As the demand for higher integration, speed, and thermal efficiency grows, glass substrates are poised to become a foundational enabler of future packaging solutions—unlocking new possibilities for AI, HPC, and beyond.

Bio:

Dr. Sung Jin Kim is the Chief Technology Officer of Absolics, a U.S.-based semiconductor packaging company spun off from SK Group. With over 30 years of experience in the semiconductor and microelectronic packaging industry, Dr. Kim spearheads the development of advanced packaging technologies and drives strategic business innovation at Absolics.

Prior to joining Absolics, Dr. Kim held executive leadership roles across a range of prominent organizations and international locations, including SKC, the Georgia Institute of Technology, Foxconn Advanced Technology, Daeduck Electronics, UTAC, and Amkor Technology. His extensive expertise encompasses package engineering, substrate manufacturing, and embedded component packaging technologies.

Dr. Kim is the holder of more than 200 U.S. patents and earned his Ph.D. in Electrical Engineering from the Technical University of Dresden in Germany.

Professional Development Course

Thursday, 23rd Oct.15:10-18:10

Dr. Kuan-Neng Chen

Dean of International College of Semiconductor Technology and Chair Professor at Institute of Electronics at National Yang Ming Chiao Tung University (NYCU), Taiwan

PDC 1

Topic: 3D IC and Advanced Packaging: Fundamentals, Hybrid Bonding, Innovations and Future Perspectives

Chair: Lewis Huang Senju Electronic (Taiwan) Co.,Ltd

Room 504C, TaiNEX 1

Outline

- Introduction to 3D IC and Advanced Packaging
- Main Schemes and Platforms
- Key Technologies and Fabrication
- Bonding and Hybrid Bonding
- Innovations and Research Achievements
- Applications, Current Status, and Challenges
- Future Perspectives

Instructor's Biography

Dr. Kuan-Neng Chen is Dean of International College of Semiconductor Technology and Chair Professor at Institute of Electronics at National Yang Ming Chiao Tung University (NYCU) in Taiwan. He received his Ph.D. degree in Electrical Engineering and Computer Science, as well as his M.S. degree in Materials Science and Engineering, both from Massachusetts Institute of Technology (MIT). Dr. Chen has held several prominent positions including Vice President for International Affairs, Associate Dean of International College of Semiconductor Technology at NYCU, Program Director of the Micro-Electronics Program at National Science and Technology Council in Taiwan, Adjunct R&D Director at Industrial Technology and Research Institute (ITRI), and Research Staff Member at IBM Thomas J. Watson Research Center.

Dr. Chen has received numerous awards and honors throughout his career, including IEEE EPS Exceptional Technical Achievement Award, IMAPS William D. Ashmon – John A. Wagnon Technical Achievement Award, Simon M. Sze Heritage Lecture, National Industrial Innovation Award, MOST/NSTC Outstanding Research Award (twice), MOST/NSTC Futuristic Breakthrough Technology Award (twice), Pan Wen Yuan Foundation Outstanding Research Award, CIE Outstanding Professor Award, CIEE Outstanding Professor Award, and IBM Invention Achievement Awards (5 times). He has authored over 400 publications, including 3 books and 7 book chapters, and holds 88 patents. Dr. Chen served as Guest Editor for the MRS Bulletin, IEEE Transactions on Components, Packaging, and Manufacturing Technology, and Materials Science in Semiconductor Processing, and has held leadership roles in various conferences and committees, such as IEEE IITC General Chair. Dr. Chen is Fellow of National Academy of Inventors (NAI), IEEE, IET, IMAPS, and CIEE and member of Phi Tau Phi Scholastic Honor Society.

Additionally, Dr. Chen is Specially Appointed Professor at Institute of Tokyo Science (previously Tokyo Tech). His current research interests focus on three-dimensional integrated circuits (3D IC), advanced packaging, and heterogeneous integration.

Thursday, 23rd Oct.15:10-18:10

Professor Andrew Tay

Singapore Hybrid-Integrated Next-Generation μ-Electronics (SHINE) Centre
Department of Electrical and Computer Engineering
National University of Singapore

PDC 2
Topic: Analysis of Fracture and Delamination in Microelectronic Packages

Chair: Andreas Ostmann, Fraunhofer IZM

Room 502, TaiNEX 1

Course Objectives

Fracture and delamination are two of the most common and persistent issues affecting the reliability of microelectronic packages. The main objective of this course is to provide a fundamental understanding as well as proven techniques of applying the fracture mechanics methodology to predicting fracture and delamination in microelectronic packages. The mechanism of popcorn cracking failure will be described and analysed. Simulation of heat transfer and moisture diffusion processes occurring during package qualification and reflow will be described. An introduction to the fundamentals of interfacial fracture mechanics will be given together with descriptions of some numerical methods of calculating fracture mechanics parameters. Experiments which verify the methodology for predicting delamination in packages will be described followed by some case studies.

Course Outline

1. Mechanical Properties and Failure of Materials.
2. Hygrothermal Stresses in Microelectronics Packages.
3. Finite Element Analysis and Stress Singularities.
4. Fundamentals of Fracture Mechanics Methodology.
5. Determination of Fracture Mechanics Parameters.
6. Measurement of Fracture Toughness.
7. Experimental Verification of the Fracture Mechanics Methodology.
8. Case Studies on delamination of pad-encapsulant interfaces, die-attach layers and on-chip interconnect structures (BEOL).
9. Cohesive Zone Modelling of Delamination and Case Studies.

Who Should Attend

This course is designed for packaging design engineers who perform reliability analysis of microelectronics and photonics packages, and anyone who wishes to understand how delaminations and fracture in microelectronics packages may be analysed.

Instructor's Biography

Dr Andrew Tay is currently an Adjunct Professor in the Department of Electrical and Computer Engineering, National University of Singapore (NUS) and a Visiting Scientist at the Singapore Hybrid-Integrated Next-Generation μ-Electronics Centre (SHINE), NUS. Prior to this he was a Professor of Mechanical Engineering at NUS. He obtained his B.E. (Hons I and University Medal) and PhD in Mechanical Engineering from the University of New South Wales, Australia. His research interests include electronics packaging (thermo-mechanical failures, delamination, effects of moisture, solder joint reliability); thermal management of electronic systems and EV batteries, infrared and thermo-reflectance thermography, solar photovoltaics reliability, and fracture mechanics.

He is currently a member of the Board of Governors of the IEEE Electronics Packaging Society (EPS), the EPS Director of Chapter Programs, and a Distinguished Lecturer of EPS. He was the inaugural General Chair of the 1st Electronics Packaging Technology Conference (EPTC) in 1997 and currently the Chairman of the EPTC Board. He was awarded the 2019 IEEE EPS David Feldman Outstanding Contribution Award, the 2012 IEEE CPMT Exceptional Technical Achievement Award, and the 2012 IEEE CPMT Regional Contributions Award. For his outstanding contributions in the application of engineering mechanics to electronics and/or photonics packaging, he was awarded the ASME EPPD Engineering Mechanics Award in 2004. He was also awarded an IEEE Third Millennium Medal in 2000. He is a Fellow of ASME and a Life Fellow of IEEE.

SESSION INTRODUCTION

ORAL PRESENTATION

SESSION 1: Strategic Breakthroughs in High-Density Server Design: Elevating Compatibility and Performance (Intel)
Time: 13:00-15:00, Oct 21, 2025
Chair: George Chen, Intel Room: 504a
Falconee Lee, Intel

Time	Topic	Lead Author	Affiliation
13:00-13:25	Design Challenges on AI System Headnode	Gerry Juan	Intel
13:25-13:50	Thermal Design Considerations for High-Density DIMM System in Dual-Socket Datacenter Server Platforms	Jay Wu	Intel
13:50-14:15	Strategic Initiative with VIPPO Technology for High-Density DDR Configuration in Next-Generation 19-Inch Server Rack Design	Thonas Su	Intel
14:15-14:40	Rack System Power Loss Analysis and Recommendation	Bryant Tsai	Intel
14:40-15:00	Electrical Characterization of High-Speed Raw Cables in Peripheral Component Interconnect Express (PCIe) 5.0 and Beyond	Ryan Chang	Intel

SESSION 2: Enabling AI and HPC: Technology Inflections Across Advanced Packaging and Interconnect (MKS' Atotech)
Time: 13:00-15:00, Oct 21, 2025
Chair: Daniel Schmidt, MKS' Atotech   Room: 504b
Eddy Chen, MKS' Atotech

Time	Topic	Lead Author	Affiliation
13:00-13:20	Future of AI hardware enabled by advanced packaging	Daniel Ng	AMD
13:20-13:40	Advanced Packaging: unleashing the true potential of semiconductor chips	Bora Baloglu	Intel
13:40-14:00	Next generation IC substrates to address emerging challenges	Venkata Mokkapati	AT&S
14:00-14:15	Advancing Redistribution Layer Plating for enhanced Reliability and Performance	Christian Ohde	MKS' Atotech
14:15-14:30	Silicon to PCB key Technology inflections impacting advanced packaging.	Kuldip Johal	MKS' Atotech
14:30-15:00	Panel Discussion	Hosted by Daniel and Eddy	

SESSION 3: Component to System-Level Integration (GEA)
Time: 13:00-15:00, Oct 21, 2025
Chair: Devan (Mahadevan) Iyer, GEA

Room: 504c

Time	Topic	Lead Author	Affiliation
13:00-13:10	Session Introduction & Advanced Electronic Packaging Program at GEA	Devan (Mahadevan) Iyer	GEA
13:10-13:40	Keynote speaker : Next Generation AI: The Importance of System Level Architecture	Raja Swaminathan	AMD
13:40-14:05	Hi HI	CP Hung	ASE
14:05-14:30	Substrates & PCBs for Chiplet packaging	Dennis (Tiang-Hao) Lin	Kinsus Interconnect Technology Corp.
14:30-14:55	Challenge and Improvement Opportunities for Large BGA Assembly	Ander Hsieh	Wistron

SESSION 4: Cu-Cu & Hybrid Bonding
Time: 13:00-15:00, Oct 21, 2025
Chair: Jenn-Ming Song, National Chung Hsing University   Room: 503
Shih-kang Lin, National Cheng Kung University

Time	Paper Code	Topic	Lead Author	Affiliation
13:00-13:30	invited	Fine-grained Cu for ultra-fine pitch Cu-Cu hybrid bonding	Chih Chen	National Yang Ming Chiao Tung University
13:30-13:45	AS0078	Effect of Water Permeation in Polyimide Materials on Polymer Hybrid Bonding	MASAO TOMIKAWA	Toray Industries Inc.
13:45-14:00	TW0076	Characterization of Cu Expansion by Variable Temperature Atomic Force Microscopy for Fine-Pitch Cu/SiO2 hybrid joints	Po-Chih Chang	ITRI
14:00-14:15	AS0118	Ultra-fast correlative metrology for hybrid bonding process of advanced package : Integrating Interferometry with Active Probe Scanning Probe Microscopy	Joonho You	nexensor Inc.
14:15-14:30	TW0114	Effect of O_2 Plasma and Citric Acid Surface Treatments on Cu/Polyimide Hybrid Bonding Reliability	Heng-Ching Mie	National Cheng Kung University
14:30-14:45	TW0081	Effect of Transition Metal Co-Electroplating on the Thermal Stability of Nanotwinned Copper Films	Chih-Chi Tsai	National Yang Ming Chiao Tung University
14:45-15:00	TW0134	Recess Depth Control by Chemical Mechanical Planarization (CMP) and Thermal Expansion Behavior of nanotwinned Cu vias in SiCN dielectrics	Chih-Hsin Tu	NYCU

SESSION 5: Advanced Characterization & Materials Behavior in Electronic Packaging
Time: 13:00-15:00, Oct 21, 2025
Chair: Alex King, Taimide Tech. Inc.
Kuo-Chan Chiou, ITRI/MCL
Room: 502

Time	Paper Code	Topic	Lead Author	Affiliation
13:00-13:30	invited	Trends in Advanced Packaging Materials and Localization Opportunities	Teng -Kuei Chen	Wafer Chem
13:30-13:45	AS0108	In-Situ Synchrotron Study of Electric Current–Driven Lattice Distortion in Au Strip for Advanced Packaging	Shubhayan Mukherjee	National Cheng Kung University
13:45-14:00	TW0215	Plasticity Effect of Annealed Cu Layers in AMB Substrates on Process-induced Warpage Behavior of SiC Power Modules	Wen You Jhu	Feng Chia University
14:00-14:15	AS0231	Materials Design of Elastomer-based Electrically Conductive Pastes for Printing Stretchable Wires Considering the Effect of their Viscoelasticity	Masahiro Inoue	Gunma University
14:15-14:30	TW0224	Effect of Copper Oxidation on the mmWave Antenna Performance	Yu-Hsun Chang	Yuan Ze University
14:30-14:45	AS0119	Advanced synchrotron and electron microscopy techniques for the development of Pb-free solder alloys and intermetallics: Case studies	Kazuhiro Nogita	The University of Queensland
14:45-15:00	TW0209	Integrating machine learning and surface characterization for predicting the mechanical performance of Cu–Cu direct bonded joints	Chun-Kai Lin	National Chung Hsing University

SESSION 6: AMD Server Solution Customer SI+EV Enablement (AMD)
Time: 15:30-17:30, Oct 21, 2025
Chair: Hellen Lo, AMD
YL Li, AMD
Room: 504a

Time	Topic	Lead Author	Affiliation
15:30-16:00	Signal Integrity Considerations for Breakout Routing and Layer Assignment in 128 Gbps PCIe 7.0 Channels	Cooper Li	AMD
16:00-16:30	A New Validation Methodology of CPU Breakout Design Trade-off	Katie Tsai	AMD
16:30-17:00	Crosstalk Impact on High-Density PAM4 SerDes PCB Breakout and Mitigation	Jun Wei Chan	AMD
17:00-17:30	Integration of DDR DIMM Connector and PCB Models for Improved Accuracy and Performance: Achieving a One Speed Bin Increase	Aik Hong Tan	AMD

SESSION 7: AI Packaging Supply Chain Ecosystem & Driving Technology (Applied Materials)
Time: 15:30-17:30, Oct 21, 2025
Chair: Albert Lan, Applied Materials
Room: 504b

Time	Topic	Lead Author	Affiliation
15:30-15:35	Session Introduction	Albert Lan	Applied Materials
15:35-15:40	Opening Remarks	Vincent DiCaprio	Applied Materials
15:40:16:05	Keynote speaker : Advancing AI with Energy Efficient Strategies	Deepak Kulkarni	AMD
16:05-16:30	Keynote speaker : Advanced Substrate for High Performance Heterogeneous Integration	Yu Hua Chen	Unimicron Technology Corp.
16:30-16:50	Panel tool (PVD/ ETCH)	Naresh Kumar Asokan	Applied Materials
16:50-17:10	Enabling AI-Era High Performance Computing with Digital Lithography	Jang Fung Chen	Applied Materials
17:10-17:30	Advanced Packaging M&I Challenges addressed by Electron Beam Technology	Bernhard Mueller	Applied Materials

SESSION 8: Thermal-Mechanical Modeling & Simulation I
Time:15:30-17:45, Oct 21, 2025
Chair: Kuo-Ming Chen, UMC　　　　Room: 504c
Yan-Cheng Liu, ITRI

Time	Paper Code	Topic	Lead Author	Affiliation
15:30-16:00	invited	Heterogeneous Integration for Malaysia's Semiconductor Leap: A Regional Partnership Opportunity	Shaw Fong Wong	Intel
16:00-16:15	AS0159	Mechanical Reliability of SiCN-Ultra Low k Dielectrics in BEOL Interconnect Depending on Fracture Mode	Yeong Seok Ham	Korea Advanced Institute of Science and Technology (KAIST)
16:15-16:30	TW0085	Evaluating Packaging Substrate Reliability and Warpage Under Thermal Conditions Referenced to Build-up Film Tg	Ming-chun Hsieh	Flexible 3D System Integration Laboratory, SANKEN, the University of Osaka
16:30-16:45	TW0084	Warpage Simulation of Automotive Modules with Metal Shielding Structure	Shen-Yu Yang	WNC Corporation
16:45-17:00	TW0046	Structural Design and Reliability Simulation of The Epoxy Flux Reinforcement Technology	You-Yi Zheng	National Tsing Hua University
17:00-17:15	TW0135	Improving Board-Level Reliability of Large BGA Packages via Edgebond Placement	Simon Chang	Zymet, Inc
17:15-17:30	TW0090	Reliability Assessment of Advanced Fan-Out Packages Under Drop Impact Conditions	Mengkai Shih	National Sun Yat-sen University
17:30-17:45	TW0232	Optical Measurement–FEA Hybrid Modeling for Thermomechanical Stress Analysis in TGV Substrates	Jui-Chang Chuang	ITRI/NTHU

SESSION 9: Interconnections & Nanotechnology
Time: 15:30-17:45, Oct 21, 2025
Chair: Chien-Lung Liang, NTUST
Takayuki Ohba, Institute of Science Tokyo

Room: 503

Time	Paper Code	Topic	Lead Author	Affiliation
15:30-16:00	invited	TSV	Takeshi Momose	Kumamoto University
16:00-16:15	US0116	Copper Interfacial Engineering for Oxide-Suppressed, Fluxless Cu-Solder and Cu-to-Cu Thermocompression Bonding	Oliver Chyan	University of North Texas
16:15-16:30	TW0169	Processing Window of Post-Treatment Room Temperature Storage Time in Low-Temperature Nanocrystalline Cu Bonding	Chen-Ning Li	National Yang Ming Chiao Tung University
16:30-16:45	AS0059	Conformal Sn Coating on Nanotwinned Cu RDLs via Immersion Plating for Reliability Enhancement	Jing Chok	National Yang Ming Chiao Tung University
16:45-17:00	TW0205	Enhancing Al–Al Ultrasonic Bonding via VUV-Induced Surface Modification in Oxalic Acid Atmosphere	Yi-Jun Hsiao	National Chung Hsing University
17:00-17:15	AS0037	Comprehensive Interface Adhesion Characterization for Advanced Semiconductor Packaging	Dong Jun Kim	Korea Advanced Institute of Science and Technology / SAMSUNG Electronics / Seoul National University of Science and Technology
17:15-17:30	TW0041	Fabrication of Fine-Grained Cu with (111)-Dominant Orientation for Low-Temperature Cu–Cu Bonding	Ke-Wei Hsieh	National Yang Ming Chiao Tung University
17:30-17:45	AS0004	Influence of Aluminum Bond Pad Characteristic toward Wire Bond Intermetallic Compound Growth	Lee Kuan Fang	X-FAB Sarawak Sdn. Bhd.

SESSION 10: Metallization & Advanced Substrate Process Integration
Time: 15:30-17:45, Oct 21, 2025
Chair: Michael Chang, Qnity™, DuPont Electronics
Shan-Jen (Simon) Kuo, Cymmetrik
Room: 502

Time	Paper Code	Topic	Lead Author	Affiliation
15:30-16:00	invited	Examination of Panel-Level Manufacturing Methods for Glass Core Substrates	Shun Mitarai	Sony Semiconductor Solutions Corporation
16:00-16:15	EU0029	Innovative Electrolytic Flash Copper Plating Equipment for Enhanced mSAP Via Reliability and Efficiency	Tobias Spoonholz	MKS Instruments / Materials Solutions Division / Atotech Deutschland GmbH & Co. KG
16:15-16:30	TW0040	Fabrication of High-Strength and High Thermal Stability Nanotwinned Copper Foils via Addition of Manganese Containing Inhibitor	PO-JUI SU	National Yang Ming Chiao Tung University
16:30-16:45	EU0161	A STUDY OF THE IMPACTS OF CURRENT DENSITY ON HIGH ASPECT RATIO THROUGH HOLES USING A NOVEL MODULAR VERTICAL ELECTROLYTIC COPPER PLATING TOOL	Gustavo Ramos	GreenSource Engineering
16:45-17:00	TW0220	Empowering the Next-Generation Design in Substrate-like PCB (SLP) and mSAP Process with DuPont™ Microfill™ LVF-7 acid copper: A Copper Electroplating Solution Offering Superior Pattern Uniformity and Unmatched Trench Via Filling	Tim Lin	DuPont
17:00-17:15	US0211	Laser Trenching (LLV) - Leveraging AODs for quality and productivity	Chris Ryder	MKS Inc.
17:15-17:30	EU0166	A Modular Electroless Copper Bath System for SAP Applications	Laurence John Gregoriades	MKS Inc.
17:30-17:45	US0038	Direct Metallization Technology Advancements	Carmichael Gugliotti	MacDermid Alpha Electronic Solutions

SESSION 11: Advanced Packaging and Metrology Technologies (ICEP)
Time: 10:10-12:10, Oct 22, 2025
Chair: Yasumitsu Orii, Rapidus　　Room: 504a
Yasuhiro Morikawa, ULVAC, Inc.

Time	Topic	Lead Author	Affiliation
10:10-10:34	Dynamic recrystallisation and crack propagation in a Sn-3Ag-0.5Cu/Cu solder joint: Development of in-situ observation of joint failure	Kazuhiro Nogita	The University of Queensland
10:34-10:58	Wafer-level Cu-Cu Hybrid Bonding and Wafer Warpage Impact	Yukako Ikegami	Sony Semiconductor Solutions Corporation
10:58-11:22	Lower inductance of POL double layer facing structure power module	Takumi Yumoto	SHINKO ELECTRIC INDUSTRIES CO, LTD
11:22-11:46	Total Solution for Particle-Free Plasma Dicing in 3D Hybrid Bonding Applications	Toshiyuki Takasaki	Panasonic Connect Co., Ltd,
11:46-12:10	Polysilazane-induced Wafer Bonding at Room Temperature and its Charactersitics	Kai Takeuchi	Tohoku University

SESSION 12: Fusion Interconnect of Electrical and Optic for Energy Efficiency (ASE)
Time: 10:10-12:10, Oct 22, 2025
Chair: CP Hung, ASE Room: 504b
Alex Wang, ASE

Time	Topic	Lead Author	Affiliation
10:10-10:40	Advance Package solution for Silicon Photonic application	Scott Chen	ASE
10:40-11:10	Advanced chiplet packages with high density interconnect for AI era	Akihiro Horibe	IBM
11:10-11:40	Advancing Co-Packaged Optics with Multi-Fiber, Multi-Color Silicon Photonics	Yung-Jr Hung	National Sun Yat-sen University
11:40-12:10	Meta Lens Arrays Enabling Scalable Co-Packaged Optics	Paul Wu	AuthenX Inc.

SESSION 13: Heterogeneous Integration
Time: 10:10-12:10, Oct 22, 2025
Chair: Shin Puu Jeng, Applied Materials
Kathy Yan, TSMC

Room: 504c

Time	Topic	Lead Author	Affiliation
10:10-10:40	Challenges in Developing Energy Efficient AI Packages: What Are the Options?	Jan Vardaman	TechSearch International
10:40-11:10	Silicon Manufacturing and Packaging at Microsoft in the Cloud/AI Era	Terrence Tan	Microsoft
11:10-11:40	Future AI Packaging Challenges and Silicon as an Integration Platform	Suresh Ramalingam	Applied Materials
11:40-12:10	Fine pitch high density RDL package	Kathy Yan	TSMC

SESSION 14: Thermal-mechanical Modeling & Simulation II
Time: 10:10-12:10, Oct 22, 2025
Chair: Sheng-Jye Hwang, National Cheng Kung University
Ming Yi Tsai, Chang Gung University
Room: 503

Time	Paper Code	Topic	Lead Author	Affiliation
10:10-10:40	invited	AI surrogate modeling and its application on PBGA reliability design	Cadmus Yuan	Feng Chia University
10:40-10:55	AS0196	Warpage Evaluation of Double-Stacked 3D Structure Using a Waffle Wafer	Wataru Doi	Institute of Science Tokyo, Kanagawa, Japan. / Murata Manufacturing Co., Ltd. Kyoto, Japan
10:55-11:10	TW0160	Reliability Characterization of Vacuum Printable Compound for SiP Encapsulation in Wireless Connectivity	CHAO-HSUAN WANG	Miniaturization Competence Center(MCC) of USI
11:10-11:25	AS0218	Inverse Analysis of Shear Fracture Characteristics for the PI-Cu Interface in Wafer-Level Packaging RDL	Hualong Fu	Institute of Microelectronics of the Chinese Academy of Sciences
11:25-11:40	TW0156	Warpage Optimization of Manufacturing Process for Fan-out Chip on Substrate-Bridge	Chung-Hang Lai	Advanced Semiconductor Engineering, Inc
11:40-11:55	TW0104	GOOD RELIABILITY FOPLP WITH DIGITAL DYNAMIC CORRECTION FOR DIE SHIFT COMPENSATION	Terry Wang	Industrial Technology Research Institute (ITRI)
11:40-12:10	TW0115	High-Performance Microfluidic Cooling for 400 W-Class ASICs in Advanced Packaging Using Au–Au Bonded Channel Structures	Yuhao Lo	National Cheng Kung University

SESSION 15: Power Electronics
Time: 10:10-12:10, Oct 22, 2025
Chair: Chang Chun Lee, National Tsing Hua University
Chun-Kai Liu, ITRI
Room: 502

Time	Paper Code	Topic	Lead Author	Affiliation
10:10-10:40	invited	Thermal and Failure Analysis of Advanced Microelectronic Devices	Andrew Tay	National University of Singapore
10:40-10:55	AS0018	Dynamic Switching Characterization of GaN Power Transistors Using Double Pulse Test (DPT) in a Fly-Buck Converter	Susmita Mistri	National Yang Ming Chiao Tung University
10:55-11:10	TW0228	Effects of Laser Scribing Parameters on the Dicing Quality of 4H-SiC	Bo-Shiuan Li	Department of Mechanical & Electro-mechanical Engineering, National Sun Yat-sen University
11:10-11:25	AS0077	Thermo-oxidation Effect on the Tensile Mechanical Properties of the Epoxy Molding Compounds at Elevated Temperature	Ayumi Saito	ROHM Company Ltd.
11:25-11:40	TW0122	Optimization of Power Module Design Based on Physical Modeling	Ji-Min Lin	Universal Scientific Industrial Co., Ltd
11:40-11:55	AS0021	The Improved Lifetime of Anisotropically Porous Pressurized Sintered Silver Die Attach	Keisuke Wakamoto	ROHM Company Ltd.
11:40-12:10	TW0126	A Modified Lifetime Prediction Model for Power Cycling Reliability of SiC Power Modules Considering Chip Size Effects	Ji-Yuan Syu	Industrial Technology Research Institute

SESSION 16: Bonding, Dielectric Materials, and Laser-Material Interactions
Time: 10:10-12:10, Oct 22, 2025
Chair: Irving Lee, Rational Precision Industry Co.,Ltd. Room: 501
Peter Chang, MacDermid Alpha Electronics Solutions

Time	Paper Code	Topic	Lead Author	Affiliation
10:10-10:40	invited	EMC Solutions Aligned with AI-Driven High-Speed/ High-Frequency Material Trends	Chieh-Sen Lee	EMC
10:40-10:55	US0233	Integrated Beam Characterization and Z-Axis Control for Enhanced Laser Focus in FPCB Via Drilling	Jack Rundel	MKS Inc
10:55-11:10	TW0206	Effects of light exposure under different atmospheres on PI-to-PI direct bonding	Mu-Jung Lin	National Chung Hsing University
11:10-11:25	EU0176	Tuning of through glass via (TGV) shapes for glass-core substrates	Valeria Samsoninkova	RENA Technologies GmbH
11:25-11:40	TW0124	Composite Perovskite Dielectrics with Temperature-Stable High-Q Performance for 5G Components	Yu-Hsuan Tseng	National Yunlin University of Science and Technology
11:40-11:55	AS0223	SPECTROSCOPIC INVESTIGATION OF FORMIC ACID TREATED COPPER SURFACES FOR DIRECT BONDING APPLICATIONS	Sarim Khan	National Chung Hsing University
11:40-12:10	TW0105	Investigating Copper oxide stability in TCB Cu-Cu bonding	Kun-Yuan Zeng	National Cheng Kung University

SESSION 17: Redefining Advanced Packaging with Glass Core Solution (Hi-CHIP)
Time: 13:00-15:00, Oct 22, 2025
Chair: Jerry Wang, ITRI   Room: 504a
Randy Wu, ITRI

Time	Topic	Lead Author	Affiliation
13:00-13:30	System on Module on Glass Substrate(SoMoG)	Li-Cheng Shen	USI Inc.
13:30-14:00	Insights from TGV Interposer Process Development	Alex Liu	Raytek Semiconductor Inc.
14:00-14:30	Trend, Opportunity & Challenge for Glass core substrate	Wen Liang Yeh	Unimicron Technology Corp.
14:30-15:00	Next Generation Interconnection by Glass Core Substrate (System on Module with Glass)	Jeng Ting Li	Unimicron Technology Corp.

SESSION 18: Enhanced Energy Efficiency in AI: Advanced Packaging and PCB Technologies for Sustainable Innovation (Qnity™, DuPont Electronics)

Time: 13:00-15:00, Oct 22, 2025

Chair: Lucy Wei, Qnity™, DuPont Electronics
Steven Lin, Qnity™, DuPont Electronics

Room: 504b

Time	Topic	Lead Author	Affiliation
13:00-13:15	Opening: Qnity™ - Powering the Next Leap Forward	Lucy Wei	Qnity™, DuPont Electronics
	Opening: Qnity™ – Powering the Next Leap Forward	Steven Lin	Qnity™, DuPont Electronics
13:15-13:45	The Evolution of Chip Package Interaction (CPI) Considerations and Technology Impact in Packaging and Assembly	Andrew Yeoh	Taiwan Semiconductor Manufacturing Company
13:45-14:15	Advanced Packaging Challenges and Opportunities	Shin Puu Jeng	Applied Materials Singapore Technology Pte. Ltd.
14:15-14:35	One-Bath Electroplating for All Layers in Chip-Scale-Packaging: Empowering Edge Mobile and AI	Chieh-Ju Li	Qnity™, DuPont Electronics
14:35-15:00	DuPont Advanced Flex Technologies For AI, Cloud, and Edge Computing	Michael Chang	Qnity™, DuPont Electronics

SESSION 19: Deep Learning for Geometry & Mechanics Prediction
Time: 13:00-15:00, Oct 22, 2025
Chair: Shu-Shen Yeh, Google Room: 504c
Cadmus Yuan, Feng Chia University

Time	Paper Code	Topic	Lead Author	Affiliation
13:00-13:15	AS0008	AI-Enabling the Solder Height Prediction	Law Yi Kei Owen	Nexperia Hong Kong
13:15-13:30	TW0132	Effect of Process Parameters and Their Interactions on Packaging Process in System in Package Structure	Sheng-Jye Hwang	National Cheng Kung University
13:30-13:45	AS0033	Pattern Shapes Prediction in Cross-sectional Images and Proposing Processes with Neural Network	Kohei Motojima	TAIYO HOLDINGS CO., LTD.
13:45-14:00	TW0178	Hybrid Machine Learning-Based Warpage Prediction for Fan-Out Panel Level Packaging	Ya-Chi Chen	National Tsinghua University
14:00-14:15	TW0235	Improving Substrate Warpage Control in Flip Chip Bonding via Optimized Cover Jig Design with Reinforcement Learning	Chi-Hua Yu	National Cheng Kung Univeristy
14:15-14:30	TW0188	Parallel-Accelerated Neural Network-Based Lifetime Prediction and Design Optimization for Wafer-Level Packages Using Finite Element Simulation	Chang-Hsu Lo	National Tsing Hua University
14:30-14:45	TW0139	Warpage Behavior Prediction of Multi-layer RDL in Fan-out Wafer-level Packaging Based on Artificial Neural Networks	Sheng-Jye Hwang	National Cheng Kung University
14:45-15:00	TW0050	Mechanistic Study of CMP Retainer Rings for Wafer-Edge Integrity	You-Sheng Song	National Sun Yat-sen University

SESSION 20: Advanced Materials, Automatic Process & Assembly
Time: 13:00-15:00, Oct 22, 2025
Chair: Lewis Huang, Senju Electronic (Taiwan) Co.,Ltd Room: 503
Kwang-Lung Lin, National Cheng Kung University

Time	Paper Code	Topic	Lead Author	Affiliation
13:00-13:30	invited	Key Enabling of Memory Packaging Materials for Future AI High Performance Computing & Humanoid Robots	Chong Leong Gan	Micron
13:30-13:45	AS0036	A liquid epoxy encapsulant with excellent weather resistance, long-term reliability and casting properties	Satoshi Osawa	NIHON GOSEI KAKO co., Ltd.
13:45-14:00	EU0201	A next generation non etching adhesion promoter enabling streamlined process for Advanced IC substrates	Thomas Thomas	MKS Atotech Taiwan Limited
14:00-14:15	TW0141	Study of Copper Particle Precipitation on BGA Solder Balls in Reflow Processes	Kuan-Cheng Liu	Siliconware Precision Industries Co. Ltd.
14:15-14:30	AS0010	Adhesives for high coupling efficiency photonic packaging	lim, see chian Garian	DELO Industrial Adhesives
14:30-14:45	TW0047	Fan-out RDL process and shuttle service	Chenchun Yu	Electronics and Optoelectronics System Research Laboratories / Industrial Technology Research Institute
14:45-15:00	AS0145	Acceleration of Silver Micro-flake Sintering by Binder Chemistry in Flexible Epoxy-Based Conductive Adhesives for Enhancing Connection Properties	Takanori Fukushima	Graduate School of Science and Technology, Gunma University

SESSION 21: Materials and Interfaces for Reliable Electronics
Time: 13:00-15:00, Oct 22, 2025
Chair: Jimmy Hsu, Intel
Haley Fu, iNEMI
Room: 502

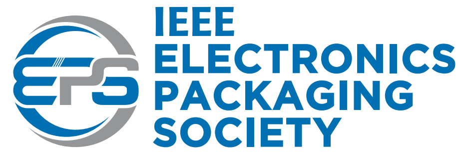
Time	Paper Code	Topic	Lead Author	Affiliation
13:00-13:45	invited	Low-Carbon Inkjet Technology from PCB and Its Potential for Semiconductors	Takato Katahira	Elephantech
13:30-13:45	AS0110	In-Situ Compression of Single-Crystal Copper Micropillars under Electric Current Stressing	Andre Cheong Kai Bin	National Cheng Kung University, Tainan, Taiwan
13:45-14:00	TW0208	Mechanical Behavior Analysis of Intermetallic Compounds in Advanced Microelectronic Solder Joints	Wei-Rong Yang	Academy of Circular Economy, National Chung Hsing University
14:00-14:15	TW0204	Evaluation of Copper Surface Oxide Constitution and Thickness on Cu-to-Cu Direct Bonding	Shih-Jie Yan	Department of Materials Science and Engineering at National Chung Hsing University
14:15-14:30	TW0198	An Electrochemical Investigation of Oxidized Copper Surface	Hui Juan He	National Chung Hsing University
14:30-14:45	TW0051	Study of Ultra-thin Structure for Flip Chip Ball Grid Array Substrate	Ye rick	Siliconware Precision Industries Co., Ltd.
14:45-15:00	TW0191	Design Sn-In-X low-temperature solder under machine learning guidance	Hao-Wei Kuo	National Cheng Kung University

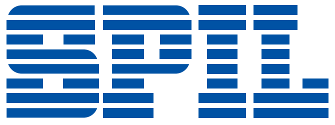
SESSION 22: Reliaiblity and Thermal Management of Advanced Packages (ISMP)
Time: 15:30-17:30, Oct 22, 2025
Chair: Taek-Soo Kim, KAIST Room: 504a
Daeil Kwon, Sungkyunkwan University

Time	Topic	Lead Author	Affiliation
15:30-15:54	High thermal conductivity materials for thermal management in electronics	Joon Sang Kang	KAIST
15:54-16:18	Understanding Thermally Induced Failures in Packaging Interconnects via Micro-scale Deformation Analysis	Tae-Ik Lee	KITECH (Korea Institute of Industrial Technology)
16:18-16:42	Synergistic metallization on advanced packages for reliable edge Ai	Hanwool Yeon	GIST
16:42-17:06	Opportunities in Advancing Packaging Technologies for Soft Electronics	Seung-Kyun Kang	Seoul National University
17:06-17:30	Analysis of microstructure effect on Cu-Cu bonding interface based on Crystal plasticity theory	Eun-Ho Lee	Sungkyunkwan University

SESSION 23: IEEE EPS: Materials and Technologies for Advanced Packaging (SPIL)
Time: 15:30-17:30, Oct 22, 2025
Chair: Shaw Fong Wong, intel
Jenn-Ming Song, National Chung Hsing University
Room: 504b

Time	Topic	Lead Author	Affiliation
15:30-16:00	Alkaline developable polyimide enabling low shrinkage and high Tg for next generation interposer	Hirokazu Ito	JSR
16:00-16:30	Empowering Region-10 Through IEEE EPS Collaborations: Innovation, Integration, and Impact	Shaw Fong Wong	intel
16:30-17:00	Light Enhanced Direct Metal Bonding for Advanced Electronic Assembly	Jenn Ming Song	National Chung Hsing University
17:00-17:30	Functional Diversification via Heterogeneous Integration	Chuan Seng Tan	Nanyang Technological University





SESSION 24: Process & Manufacturing in Advanced packaging
Time: 15:30-18:00, Oct 22, 2025
Chair: Cheng En Ho, Yuan Ze University
Rozalia Beica, Rapidus Corporation
Room: 504c

Time	Paper Code	Topic	Lead Author	Affiliation
15:30-16:00	invited	Enabling AI and HPC: Defect-Free, Co-Planar Copper via fill Plating process for Advanced IC Substrates	Sam Dharmarathna	Macdermidalpha Electronics solutions
16:00-16:15	US0026	Identifying Sub-10 μm Unknown Organic Foreign Matters by Laser-based Optical Detection of Infrared Photoinduced Localized Mirage Effect	Michael K. F. Lo	Photothermal Spectroscopy Corp
16:15-16:30	TW0179	Advanced Optical Metrology Using on Quality Monitoring of Carrier Wafer in Advanced Packaging	Mr. Ting-Wei Chen	TSMC
16:30-16:45	TW0034	Advanced Co-packaged Optics (CPO) Solutions and Technology Challenge for Silicon Photonics Applications	Mike Tsai	SPIL
16:45-17:00	US0094	Enabling Chemical Seed Etch Process for Fine-Line Cu Redistribution Layer for Microelectronic Packaging	Darko Grujicic, Ph.D.	Intel Corporation
17:00-17:15	EU0045	Tool-Agnostic Pulse Reverse Electroplating for High Aspect Ratio Through Glass Vias in Advanced Packaging	Dennis Fiedler	MKS, Materials Solution Devision, Electroplating
17:15-17:30	TW0044	Large 600 x 600 mm Panel Recon Molding Filling Improvement for New Type Epoxy Molding Compounds	Ling-Hua Wang	Advanced Semiconductor Engineering, Inc.
17:30-17:45	TW0236	ADDRESSING NEXT-GENERATION IC SUBSTRATE CHALLENGES: MKS ADVANCED LASER DRILLING OF RESONAC MATERIAL FOR HIGH-DENSITY PACKAGING	Weiming Cheng	MKS Inc.
17:45-18:00	TW0052	Low Temperature Bonding Using Nanocrystalline Copper Lightly Doped with Nickle	Hsin-Lin Kai	National Yang Ming Chiao Tung University

SESSION 25: Characterization, Testing, & Inspection in Advanced Packaging
Time: 15:30-18:00, Oct 22, 2025
Chair: Yu-Jung Huang, NKUST Room: 503
Ming Yi Tsai, Chang Gung University

Time	Paper Code	Topic	Lead Author	Affiliation
15:30-16:00	invited	Approaches for Glass Core Substrate Technologies	Andreas Ostmann	Fraunhofer IZM
16:00-16:15	AS0129	A Novel Uniaxial Tensile Test Simulating Delamination Between Resin and Metal	Masaya Ukita	ROHM Co., Ltd.
16:15-16:30	TW0053	Numerical and experimental study of wafer probing mark formation on aluminum pad with Cobra-type vertical probe needle	Hsueh-Chih Liu	Advanced Institute of Manufacturing for High-tech Innovations, National Chung Cheng University, Chiayi 621301, Taiwan
16:30-16:45	AS0136	Stochastic Physics Informed Machine Learning in Explainable Defect Detection and Prediction	Shang Yi Lim	National University of Singapore
16:45-17:00	TW0177	Effect of Geometric Nonlinearity on Biaxial Bending Strength of Thin Silicon Dies by Ring-on-Ring Test	Ming-Yi Tsai	Dept. of Mechanical Engineering, Chang Gung University, Taiwan
17:00-17:15	AS0199	Evaluation of Deformation and Strain in Cu Pillar Bumps under Compressive Loading via Digital Image Correlation Method	Masaaki Koganemaru	Kagoshima University
17:15-17:30	TW0043	A Unified GAN-Based Anomaly Detection Framework for PCB Inspection	Chao-Ching Ho	National Taipei University of Technology
17:30-17:45	TW0093	Evaluating the Impact of Ball Size and Alloy Composition on the Reliability of Lead-Free Solder Joints	Wei-Ting Lin	National Central University
17:45-18:00	TW0089	Evaluation of low thermal resistance film type TIM for FCBGA package	Pin-Jing Su	Siliconware Precision Industries Co., Ltd.

SESSION 26: Thermal characterization & Management
Time: 15:30-18:00, Oct 22, 2025
Chair: Chien Yuh Yang, National Central University Room: 502
Ben Je Lwo, National Defense University

Time	Paper Code	Topic	Lead Author	Affiliation
15:30-16:00	invited	A simple step gap design to improve the spreading performance of vapor chamber	Chi-Chuan Wang	NYCU
16:00-16:15	EU0107	Towards High Spatial Contactless Temperature Monitoring in GaN Devices Using Thermoreflectance	A. Myalitsin	ANVOS Analytics Co., Ltd.
16:15-16:30	TW0202	Thermal Performance of Hybrid Liquid Cooling for Data Center	Chun-Kai Liu	Industrial Technology Research Institute
16:30-16:45	AS0061	High-Throughput Thermal Simulation for Early-Stage 3D-IC Design Using Automated Meshing and Pseudo-3D Modeling	Kenji Ono	Kyushu University
16:45-17:00	TW0055	Enhanced Thermal Performance of Vapor Chambers with Modified Hierarchical Dendritic Wick Structures in Evaporators	Po-Hsun He	National Tsing Hua University
17:00-17:15	AS0012	Combined Lee Model Based Numerical Scheme and Analysis of Variance for Optimizing the Thermal-Hydraulic Performance of Pillar-Reinforced Vapor Chamber	Yusuf Rahmatullah	National Taiwan University of Science and Technology
17:15-17:30	TW0153	Thermal Interface Material Validation Framework for Large-Scale Chip Packages	Chris Lin	Wistron Corporation
17:30-17:45	TW0121	Transient Thermal Analysis for Packages in the Laser Assisted Bonding (LAB) Process	Bo-Yu Huang	ASE Group Chung-Li Branch
17:45-18:00	TW0234	AI-Driven Microfluidic Engineering for Advanced Thermal Control in Power-Dense Electronics	Chi-Hua Yu	National Cheng Kung University

SESSION 27: Smart Manufacturing and System Modeling
Time: 15:30-18:00, Oct 22, 2025
Chair: Takeyasu SAITO, Osaka Metropolitan University Room: 501
SJ Wu, I-Shou University

Time	Paper Code	Topic	Lead Author	Affiliation
15:30-16:00	invited	Modulization and Miniaturization for power delivery in high performance computing	Li-Cheng Shen	USI
16:00-16:15	AS0096	Warpage-Induced Signal Integrity Degradation in High-Speed PCB: A Multi-Domain Analysis and Design Framework	John Lin	Lenovo
16:15-16:30	TW0112	Accelerating AI-Based Defect Detection in Manufacturing: Synthetic Data and Model Optimization for Rapid and Stable Deployment	Wong-Shian Huang	ASE Inc.
16:30-16:45	TW0154	Automated Component Polarity Detection Image Recognition System Based On Deep Learning And Metric Learning	Ching-Ju Tsai	Universal Scientific Industrial Co., Ltd.
16:45-17:00	EU0006	Closed-Loop IIoT Control for Sustainable and Intelligent PCB Manufacturing: A Data-Driven Approach Integrating Domain Expertise	Giovanni Obino	Mks Inst
17:00-17:15	TW0226	Research on Enhancing Automated Material Handling System Performance in PCB Factories Using MCS Intelligent Assistant	Steven Wu	Mirle Automation Co.
17:15-17:30	TW0189	Modeling electromigration-induced resistance change in Sn-58Bi Solder Using Machine Learning Approach	Chi Chen	Department of Mechanical Engineering, National Chen Kung University
17:30-17:45	TW0186	Influence of Ni barrier on electromigration-induced transformation of Sn phase at cathodic interface	Chieh-Pu Tsai	National Central University

SESSION 28: Convergence or Divergence? Panel-Level Packaging Meets Heterogeneous Integration (Lam Research)
Time: 10:10-12:10, Oct 23, 2025
Chair: Herbert Oetzlinger, Lam Research Room: 504b
Frank Su, Lam Research

Time	Topic	Lead Author	Affiliation
10:10-10:40	Advancing Packaging Technology: Exploring Through Glass Vias for Glass Core Integration as an Alternative to Si Interposer	Herbert Oetzlinger	Lam Research
10:40-11:10	Convergence – Overcoming Plating Challenges: WLP to PLP	Steven Tam	MacDermid Alpha
11:10-11:40	Acid copper plating additive for dual damascene process in panel level packaging	Ryo Tanaka	Okuno chemical Industries Co., Ltd.
11:40-12:10	Advanced Equipment Innovations for AI-Centric Packaging Architectures	Chin-Hock Toh	Lam Research

SESSION 29: Process and Manufacturing in Advanced Packaging
Time: 10:10-12:10, Oct 23, 2025
Chair: Jun Mizuno, National Cheng Kung University
De-Shin Liu, National Chung Cheng University
Room: 504C

Time	Paper Code	Topic	Lead Author	Affiliation
10:10-10:40	invited	Chiplet Packaging and Design Strategies for Automotive-Grade Reliability	Takashi Matsumoto	Denso
10:40-10:55	AS0039	Back Side (BS) Grinding Process on 300mm Panel Fan-Out for High Performance Computing (HPC) Applications	Bandharla Dharani	ASE
10:55-11:10	TW0142	Investigation of Polyimide Dishing and Topography in Redistribution Layer Process	Sheng-Jye Hwang	National Cheng Kung University
11:10-11:25	EU0175	Enabling Energy-Efficient AI Systems through High-Density Glass Interposers Fabricated with Laser Induced Deep Etching (LIDE)	Nils Anspach	LPKF Laser & Electronics
11:25-11:40	TW0100	Early Zone Correction for Enhanced Overlay Precision in Next-Generation FOPLP Lithography	John Chang	Onto Innovation
11:40-11:55	TW0060	Mitigation of Grain Growth under Pressure on Nanocrystalline Cu in Cu-Cu Bonding	Ting-Chi Chen	National Yang Ming Chiao Tung University
11:55-12:10	TW0080	Effect of dual Ni(P) structure on nickel dissolution and interfacial compound formation	Ya-Hui Hsu	National Central University

SESSION 30: Electrical Characterization & Simulation
Time: 10:10-12:10, Oct 23, 2025
Chair: Tz Cheng Chiu, National Cheng Kung University
Sung Mao Wu, National University of Kaohsiung
Room: 503

Time	Paper Code	Topic	Lead Author	Affiliation
10:10-10:25	AS0152	Channel Component Design Sensitivity Study for Accuracy Enhancement In DDR5 Memory Channel Solution Analysis	Wei Jern Tan	AMD Server Platform SMTS Product Application Engineering
10:25-10:40	TW0164	Accelerating Design Innovation : Signal Integrity Prediction for Advanced FOCoS Packaging	Cheng-Yu Tsai	Advanced Semiconductor Engineering (ASE)
10:40-10:55	AS0130	Full Path PIPD Co-Simulation and Correlation with SDLE	Heng Chuan Shu	Advanced Micro Devices, Inc. (AMD)
10:55-11:10	TW0194	Key Considerations and Challenges in Post-Layout Simulation for High-Speed Interfaces on PCB Design	Yang, Tina	Intel
11:10-11:25	AS0151	Efficient and Accuracy-Enhanced DDR5 Memory Channel Electrical Modeling and Scalable Board Solution Analysis Methodology	Wei Jern Tan	AMD Server Platform SMTS Product Application Engineering
11:25-11:40	TW0020	Patterns dependent loss?	Edward Pan	Wiwynn Corporation
11:40-11:55	AS0113	Accurate Early-Stage On-Chip Decap Allocation and PDN Planning in Advanced Packaging Using Scenario-Driven Current Profiling	Kin Fei Yong	Tenasic Technology
11:55-12:10	AS0062	The Design Challenges and I/O Performance Tuning Methodology for Advance GPU System Integration	Li Wern Chew	AMD

SESSION 31: Interconnect & Interface Technologies for Advanced Electronic Systems
Time: 10:10-12:10, Oct 23, 2025
Chair: Geli Hung, ThinFlex Corporation
Tetsuya Onishi, Grand Joint technology Ltd
Room: 502

Time	Paper Code	Topic	Lead Author	Affiliation
10:10-10:40	invited	High-Speed Design Challenges: Evolution and PCB Ecosystem Enablement for Data Center and AI Applications	Jimmy Hsu	Intel
10:40-10:55	TW0227	Morphological Modification of Cu Electrodeposition in the PCB Bar-Via Structure for Thermal Module Applications	Jie-Yu Lin	Yuan Ze University
10:55-11:10	TW0197	Systematic Management of High-Speed Interconnect Discontinuities in Next-Generation Data Center Architectures	BRIAN HO	Intel
11:10-11:25	TW0221	Strategic Initiative with VIPPO Technology for High-Density DDR Configuration in Next-Generation 19-Inch Server Rack Design	ANN YEN	Intel
11:25-11:40	TW0225	FEA-based Neural Networks Estimation for Solder Lifetime in MLCC of PCB Layout Design	Zi-An Huang	Acbel Polytech Inc.
11:40-11:55	TW0147	Interfacial Reaction of Electrodeposited Gallium on Cu/Ni Substrate	Tzu-hsuan Huang	National Cheng Kung University
11:55-12:10	TW0207	Enhancement of direct bonding between PI and solder masks through surface modification	Yu-Wei Chen	National Chung Hsing University

SESSION 32: Glass Packaging
Time: 13:00-15:00, Oct 23, 2025
Chair: Tetsuya Onishi, Grand Joint Technology

Room: 504a

Time	Topic	Lead Author	Affiliation
13:00-13:30	Glass Package Trends &Technology	Tetsuya Onishi	Grand Joint Technology
13:30-14:00	Scaling the Square: Enabling Endless Heterogeneous Integration, From Cost-Driven to Cutting Edge	Frank Su	LAM RESEARCH
14:00-14:30	Enabling the Advanced Packaging industry with HVM solutions for next generation glass core substrates	Christian Buchner	SCHMID
14:30-15:00	Measuring Progress on Glass Substrates	Jan Vardaman	TechSearch International, Inc

SESSION 33: 3D Embedding
Time: 13:00-15:00, Oct 23, 2025
Chair: Weita Yang, ITRI
Yoshihisa Katoh, FUKUOKA University
Room: 504b

Time	Topic	Lead Author	Affiliation
13:00-13:24	Development and Evaluation of Build-Up Materials for Semiconductor Packaging Applications	Jyh-Long Jeng	Industrial Technology Research Institute
13:24-13:48	Analytical solution for Hybrid bonding Process Optimization	Masahiro Saito	Toray Research Center, Inc.
13:48-14:12	Recent trends in heterogeneous integration and our research results	Jun Mizuno	National Cheng Kung University
14:12-14:36	System Level Co-Design Platform for 3D SiP & 3D electronic module	Masaomi Suzuki	Zuken Inc.
14:36-15:00	Activity of IEC international standardization for 3D device embedded technology	Yoshihisa Katoh	Fukuoka University

SESSION 34: Materials & Processes for Advanced Packaging from Japan (JIEP)
Time: 13:00-15:00, Oct 23, 2025
Chair: Takeyasu SAITO, Osaka Metropolitan University Room: 504c
Hirokazu Noma, Resonac Corporation

Time	Topic	Lead Author	Affiliation
13:00-13:20	Effects of Bonding Properteis About Porous Bumps Fabricated by Electroplating Process	Takuma Nakagawa	Mitsubishi Materials Corporation
13:20-13:40	Highly dispersed and low temperature sinterable submicron copper particles	Ukyo Suzuki	Kao Corporation
13:40-14:00	Surface Activation of Cu/SiO_2 for Hybrid Bonding by 172-nm Ultraviolet Irradiation with an Excimer Lamp	Kejun Wu	Ushio Inc.
14:00-14:20	Polyimides Compositions with Good Flexibility and Low Dielectric Property Corresponding to advanced semiconductor packages using Heterogeneous Integration Technologies	Takashi Tasaki	ARAKAWA CHEMICAL INDUSTRIES, LTD.
14:20-14:40	Development of Surface treatment chemicals for interposers	Reito Kobayashi	JCU Corporation
14:40-15:00	Manufacturing Technology Solution of Panel / Wafer Level Packaging for Chiplet Integrations	Masafumi Wakai	ULVAC, Inc.

SESSION 35: Scalable Modeling in Advanced Packaging
Time: 13:00-15:00, Oct 23, 2025
Chair: Meng-Kai Shih, National Sun Yat-sen University — Room: 503
Ching-Feng Yu, National United University

Time	Paper Code	Topic	Lead Author	Affiliation
13:00-13:30	invited	A new heterogeneous infinite element method for mechanical/thermal stress analysis of three-dimensional through-silicon via structures in electronic packaging	De-Shin Liu	National Chung Cheng University
13:30-13:45	US0013	Warpage Resistance of Glass Substrate Containing Through-Glass-Vias: A Numerical Analysis	Yu-Lin Shen	University of New Mexico, U.S.A.
13:45-14:00	TW0183	Study on Multi-Point Constraints and Equivalent Beam for Reducing Simulation Time in 3D WLP	Chia-En Chang	National Tsing Hua University
14:00-14:15	TW0028	Studying of the Equivalent Beam Structure for the Reliability Prediction of the Heterogeneous Integration Module	Cadmus Yuan	Feng Chia University
14:15-14:30	TW0054	A Pixel-Based Equivalent Approach of Finite Element Model for Warpage Prediction in PCB	Chin-Hung Lai	National Cheng Kung University
14:30-14:45	TW0182	A Global-Local Finite Element Simulation Approach for Early Failure Detection in Chiplet Packaging	Wei-Fong Wang	National Tsing Hua University
14:45-15:00	TW0007	Computational Simulation of Flux Removal Efficiency in Encapsulation Devices at a 1:10,000 Scale via Two-Phase Flow Modeling	TZU CHIEH CHIEN	Advanced Semiconductor Engineering, Inc

SESSION 36: Advanced Materials & Processing for Electronic Packaging
Time: 13:00-15:00, Oct 23, 2025
Chair: Yasuhiro Morikawa, ULVAC　　Room: 502
Kuan-Jung Chung, National Changhua University of Education

Time	Paper Code	Topic	Lead Author	Affiliation
13:00-13:15	AS0117	Optimizing Vacuum Ultraviolet Irradiation Pretreatment Condition for Wet Desmear: Balancing Permanganate Time Reduction and Resin Surface Quality	Akihiro Shimizu	Ushio Inc.
13:15-13:30	US0011	Can ENIG / ENEPIG Processes be More Sustainable?	Frank Xu Ph.D.	MacDermid Alpha Electronics Solutions, Waterbury, CT, USA
13:30-13:45	TW0049	In-House Recovery of Palladium Catalysts from PCB Wastewater for Reuse in Electroless Plating	Yi-Ting Wu	National Tsing Hua University
13:45-14:00	TW0195	Optimization of Electroplating Parameters to Fabricate Nanotwinned Foils via Complex System Response Platform	Chun-Ting Ke	National Yang Ming Chao Tung university
14:00-14:15	TW0193	Light-removable surface protective layer for Cu to Cu bonding applications	Wei-Ting Chen	National Chung Hsing University
14:15-14:30	TW0172	Interfacial Reactions Between Tin and Ruthenium	Hsiu-Mei Yang	National Cheng Kung University
14:30-14:45	TW0144	Development of High-temperature Lead-free solders: Zn-Sn-Al-Cu Based Alloy	Yu-Sheng Chen	National Taiwan University of Science and Technology
14:45-15:00	TW0181	Design high shear strength Sn-Bi-X low-temperature solders on Cu substrate using a machine learning approach	Zhi-Chen Ai	National Cheng Kung University

SESSION 37: 【Open seminar】AI-Powered in Semiconductor Packaging (TPCA)
Time: 13:00-15:00, Oct 23, 2025
Chair: Albert Lan, Applied Materials

Room: 4F L-1308

Time	Topic	Lead Author	Affiliation
13:00-13:05	Opening Remarks: Overall Advanced Package Market & Technology Trend	Albert Lan	Applied Materials
13:05-13:35	Advanced package materials development for Large Panel Interposer and Large Package through co-creative evaluation platform	HIDENORI ABE	Resonac
13:35-14:05	Current trends of 3D Integrated CMOS Image Sensors	Yoshihisa Kagawa	Sony Semiconductor Solutions
14:05-14:35	Taiwan's Pressure: Possessing the Ability to Mass-Produce the World's Most Energy-Efficient AI Chips – A Geopolitical Analysis	Rocky L. Uriankhai	SciTech Power Research Ltd.
14:35-15:00	Advanced Packaging and IC substrates in the AI and HPC era	M.Bilal HACHEMI	Yole

SESSION 38: 【Open seminar】AI HW Process and Metrology : Soldering, Package, TGV and PCB (SMTA Taiwan Chapter)
Time: 15:10-17:00, Oct 23, 2025
Chair: Jeffrey Lee, SMTA Taiwan Chapter
Room: 4F L-1308

Time	Topic	Lead Author	Affiliation
15:10-15:38	Challenge of Low Temperature Soldering	Ning Cheng Lee	ShinePure Hi-Tech
15:38-16:05	Cost-Effective 3D Packaging for AI Wearables Through Embedded Die Substrate	Charles Lin	Bridge Semiconductor
16:05-16:33	An Advanced optical engine in selective laser etching (SLE) for TGV mass production	James Chien	Taiwan ForeSight Co.Ltd
16:33-17:00	PCB Pad cratering Characterization for large size AI Package.	Jeffrey Lee	Integrated Service Technology Inc.

Poster session I - Packaging

Time: 15:00-15:30, Oct21,2025
Chair: Hsien Chie Cheng, Feng Chia University
Hsiang-Chen Hsu, I-Shou University
John Liu, TPCA
Yu Po Wang, IEEE EPS

Foyer Area

Paper Code	Scope	Topic	Lead Author	Affiliation
TW0027	P1	Scalable Via Array Substrate for Programmable Packaging Applications	Tsung Yu Ou Yang	ITRI
TW0030	P1	Enhancing Electromigration Reliability in Flip-Chip Micro Bump via Pre-Heating Treatment	Chih-Yuan Chang	National Yang Ming Chiao Tung University
TW0056	P1	Design on Trapezoidal and Pyramidal Shaped Dielectric Resonator Antennas for Millimeter Wave Applications	Ruenn-Bo Tsai	National Sun Yat-sen University (NSYSU)
TW0058	P1	Quantitative Effect of Sawing-Line Width on QFN Thermal Deformation	Jie-Ming Li	National Sun Yat-Sen University
TW0063	P1	Evaluation of a New Power GaN Package Using a Flip Chip Bonding Process	Ching Kuan Lee	ITRI
TW0064	P1	Study of Silver Wire Bonding for NAND Flashes to Meet Automotive Grade	Ruenn-Bo Tsai	National Sun Yat-sen University (NSYSU)
TW0065	P1	Analysis of Copper Keep-out Impacts on Differential Pair Signal Integrity	Ruenn-Bo Tsai	National Sun Yat-sen University (NSYSU)
TW0067	P1	Evaluation and Analysis of Thermal Performance, Structural Reliability, and Insulation Capability of IMS Substrates in Power Module Applications	Tsung Han Li	ASE/NSYSU
TW0070	P1	Effect of Sintering Sequence on the Reliability of DTS-Enhanced Die Attach with Sliver Sintering Processes	BAO-LIN YE	National Sun Yat-sen University
TW0072	P1	Optimization Study on the Dog-Ear Effect in Printing Sintered Silver Paste	PO YUAN LIN	NSYSU
TW0073	P1	Cu–Cu Interconnect Reliability and Impedance Characteristics through Ultrasonic Welding and Solder Paste Bonding Techniques	BING-ZONG WU	National Sun Yat-sen University
TW0074	P1	Copper Paste Innovations for High-Performance Power Module Bonding	Chen Kuan Chih	National Sun Yat-sen University
TW0075	P1	Exploring the Thermal Dissipation Performance of High Thermal Conductivity and High Tg in Advanced Semiconductor Packaging Processes	Ming Ru Wu	National Sun Yat-sen University
TW0082	P1	Finite-Element Investigation of Wafer-Edge Stress and Deformation during Post-CMP Cleaning Vibrations	Shih-Yun Tu	National Sun Yat-Sen University
TW0097	P1	Research on the Cleaning of Multi-layer Boards By Using MW Plasma	Liu Shang-Hong	ASE(Advanced Semiconductor Engineering, Inc.)

Paper Code	Scope	Topic	Lead Author	Affiliation
AS0131	P1	Low-Roughness UV Laser Drilling for Sub-10 µm Vias in Advanced Semiconductor Package Substrates	Nam Son Park	Tech university of korea
AS0192	P1	Effect of Sn decorated MWCNT in Composite Solder Assembled by IPL energy	DongGil Kang	Sungkyunkwan university
AS0219	P1	Reliability Assessment of Cycloaliphatic Epoxy Encapsulation for Next-Generation Power Modules	Takuya Nakagiri	Osaka University
TW0083	P2	The Study and Analysis of High Glass Transition Temperature Epoxy Resin in Power Module Packaging	Tsung-Chieh Wu	National Sun Yat-sen University
TW0120	P2	Ultra-low Residue Flux Applications in Non Clean Uderfill Process	Kuo-Hua Hsieh	Wistron NeWeb Corporation
TW0128	P2	Improvement on Electrostatic Discharge Robustness of SiC VDMOSFET with Co-Packaged Transient Voltage Suppressor	MING-DOU KER	National Yang Ming Chiao Tung University
TW0146	P2	Integration of High-Temperature Sintered Via-Filling and DPC Technology for Spacer-Free Ceramic Substrates in High-Power Modules	Shih Che Shen	Tong Hsing Electronic Industries
AS0086	P3	Enhanced Mechanical Reliability of Ni-less DPIG Solder Joints via Laser Selective Reflow for Fine-Pitch Semiconductor Packaging	TAE-HYEON LEE	Korea Institute of Industrial Technology / Gyeongkuk National University
TW0162	P3	2D material-based composite with anisotropic EM and thermal characteristics for IC EMC/EMI protections	Chien-Hao Liu	National Taiwan University
TW0180	P3	ow-Warpage Organic RDL Interposer with Chip-First Hybrid Bonding Integration for 3D Heterogeneous Wafer-Level Packaging	Ching-Feng Yu	National United University
TW0184	P3	Design on Truncated-Conical and Conical Dielectric Resonator Antennas for Millimeter Wave Applications	Ruenn-Bo Tsai	National Sun Yat-sen University (NSYSU)
AS0103	P6	Choline-based Ionic liquids and gels for Organic Electrochemical Transisters	Sungbin Choi	Sungkyunkwan University
TW0185	P6	Design on Hexagonal Shaped Dielectric Resonator Antenna for Millimeter Wave Applications	Ruenn-Bo Tsai	National Sun Yat-sen University (NSYSU)
TW0190	P6	Warpage Behavior and Mitigation of Power Modules Using High Tg Molding Compounds under High-Temperature Processing	Ming-Pei Lu	National Sun Yat-sen University
TW0213	P6	An Innovative dual fan-out module 3D packaging architecture for large-size, low-warpage, high-density multi-chip heterogeneous integration	Chao kai Hsu	Industrial Technology Research Institute
TW0216	P6	Electromigration reliability of micro joints with different surface coatings over Cu pads	Chih Chieh Huang	Yuan Ze University
TW0217	P6	Simulation-Driven Ensemble Learning for Process-induced Warpage Prediction in Power Electronics Packaging	Hsu Siang-yu	Feng-chia university

Poster session II - Packaging & PCB

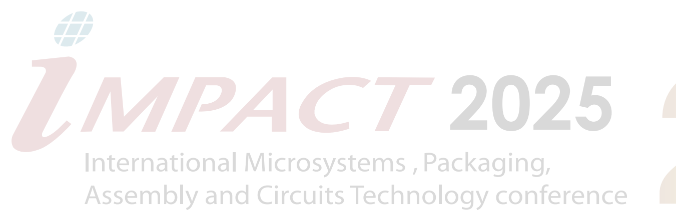
Time: 15:00-15:30, Oct22,2025
Chair: Hsien Chie Cheng, Feng Chia University
Hsiang-Chen Hsu, I-Shou University
John Liu, TPCA
Hideyuki Nishida, SMIC (Senju)

Foyer Area

Paper Code	Scope	Topic	Lead Author	Affiliation
TW0123	B1	LOW-TEMPERATURE COMPOSITES FOR 5G FILTERS WITH CO-FIRING AND GREEN MANUFACTURING POTENTIAL	Zhong Hao Wang	National Yunlin University Science and Technology
TW0171	B1	The interfacial properties of Indium thermal interface materials	Po-hsiang Juan	National Cheng Kung University
TW0187	B1	Study on the adsorption of methylene blue, methyl green, methyl orange and copper by calcium aluminum layered double hydroxides	Huan-Ping Chao	Chung Yuan Christian University
TW0212	B1	Advanced Copper Foil Development for Power Efficiency Enhancement	TSAI KE CHENG	Intel
AS0017	B2	Digitalizing SMT OEE through big data optimization and self-service analytics	JINBIAO XU	Universal Scientific Industrial Co., Ltd.
AS0019	B2	Development of Automatic inserting Jumper Cap Machine	Zhang Zhiyong	USI
TW0025	B2	Demonstration of QRcode as traceability sipID in the advanced packaging process and the transparent substrates supply chains	Fu Gow Tarntair	Minghsin University of Science and Technology
TW0098	B2	Early Detection of Electromigration-Related Lattice Instability in Au Strip	MING-WEI HUNG	National Cheng Kung University
AS0138	B3	Advanced Flat Cable Innovations for Scalable and Flexible System Architectures	Chiew Yee Ho	Intel
TW0102	B3	A Comprehensive Study of Substrate Design for High Power Applications	SHAOYU LU	TONG HSING ELECTRONIC IND. LTD
TW0133	B3	Low-Loss Build-Up Dielectric Materials for Advanced IC Substrates	wenpin Ting	Industrial Technology Research Institute
TW0149	B3	Silver thin film formation by galvanic reaction	YU HAO CHOU	National Cheng Kung university
TW0158	B3	Electrodeposited Gallium for Low- Temperature Bonding Interconnection	Huang An Yu	National Cheng Kung University (NCKU)
TW0155	B4	A Study on Frequency-Domain Feature Diagnosis Technology for Interior Permanent Magnet Synchronous Motor Control Systems Based on PCB Design	WEI XIN CHEN	National Formosa University
AS0099	P5	Next-Generation Adhesive for 3D Integration: Room-Temperature WOW/COW Bonding and Potential for Hybrid Interfaces	Naoko Araki	Daicel Corporation
AS0148	P5	Highly Thermally Conductive Packaging Underfill with Porosity-Suppressed hBN–Al_2O_3 Hybrid Spherical/Fibrous Fillers	Yeonwook Jeong	Sungkyunkwan University
TW0035	P5	Low-Frequency Noise-Based Evaluation of a-IGZO TFTs under Thermal Annealing and Fluorine Plasma for BEOL-Compatible Reliability Design	Hsin-Hui Hu	National Taipei University of Technology
TW0057	P5	High Aspect Ratio Micro-vias Drilling on Aluminum Nitride Substrates by Picosecond Laser	Ruenn-Bo Tsai	National Sun Yat-sen University (NSYSU)
TW0066	P5	Low Taper Ratio TSV by Ultrashort Pulse IR Laser Drilling	Ruenn-Bo Tsai	National Sun Yat-sen University (NSYSU)

Paper Code	Scope	Topic	Lead Author	Affiliation
TW0079	P5	Integration of High-Toughness Silicon Nitride and DPC Fine-Line Processing for High-Reliability Ceramic Substrates	Hong Yu Chang	Tong Hsing Electronic Industries, Ltd.
TW0137	P5	Electric Field Alignment of Plate-like and Polyhedral Alumina Fillers in Epoxy Composites for Enhanced Thermal Conductivity and Electrical Insulation	HAOTSE LO	Kyushu Institute of Technology
TW0163	P5	A Thin-Film Electroadhesive Component for Versatile Integration into Haptic Feedback Systems	Ching-Yu Liu	Industrial Technology Research Institute
AS0143	P2	Preparation of Dicyclopentadiene Resin-sealed power modules and comparison of power cycle tests under high temperature and high humidity environments.	NOBUHITO KAMEI	RIMTEC CORPORATION
AS0009	P4	LOCAL RESIDUAL STRESS MEASUREMENT IN THIN-FILM STRUCTURES VIA FIB-DIC: COUPLED WITH ARTIFICIAL NEURAL NETWORK MODELING	Jong-hyoung Kim	Pukyong National University
AS0092	P4	Standardization of SP7 Backplane Chassis by using small form factors and common EDSFF SSD tray	soo hin hoe	AMD Global Services (M) Sdn Bhd
AS0125	P4	Optimizing Memory Performance: Analyzing Design Influencers on Eye Margin in Advanced Computing Systems	Hann Shen Fabian Tan	AMD
AS0140	P4	Accelerating High-Speed Interconnect Development with a Closed-Loop Design and Validation Framework	Chiew Yee Ho	Intel
AS0157	P4	4D Gaussian Splashing Improved by Time-Scene Flow	HongLin Li	DongGuan University of Technology
AS0230	P4	Non-destructive interconnection reliability validation by warpage for ball grid array packages using digital image correlation	Seongkyu Choi	Korea Institute of Industrial Technology
TW0005	P4	LSTM with ETL Customer Demands and Forecast	ZongYuan Wu	USI
TW0022	P4	Design of Glass Embedded Fan Out Antenna in Packaging (FO_AiP) Using Backpropagation Algorithm	Ben-Je Lwo	National Defense University
TW0032	P4	Accelerating AI Server Design: A Cost-Effective Simulation Methodology for High-Speed I/O Verification	Dian-Ying Wu	Intel
TW0091	P4	Mechanical Stress Analysis of Small BGA on Translation Boards Under Temperature Cycling Test Conditions	Zhan-Ying Guo	NXP
TW0101	P4	Reliability ant Thermal Challenges for High Thermal TIM Materials	ICheng Huang	ASE
TW0173	P4	Cross-Ratio Formulation of Two-Line Method for Charactering Wideband Propagation Constant of Transmission Lines	Kuen-Fwu Fuh	National United University
TW0214	P4	Interaction of debonding crack and the RDL Cu trace in a 2.5-D package under temperature cycling condition	Tz-Cheng Chiu	National Cheng Kung University
AS0150	P7	Development of Aligned AlN Nanofiber-Based Anisotropic Thermal Films for Enhancing the Output Performance of Flexible Thermoelectric Generators: Experimental and FEM Simulation Study	Jungbin Shin	Sungkyunkwan University
AS0229	P7	Oxidation-Inhibited Cu Direct Bonding via Glucose Vapor for Green Semiconductor Packaging	Nahye Kim	Korea Institute of Industrial Technology
TW0015	P7	Formic Acid Vacuum Reflow with Flux-free Solder Paste Process Evaluation in SiP Module	Chih Yen Chen	USI, Universal Scientific Industrial
TW0023	P7	Integrated Design and Simulation of a Thermoformed Central Control Console for Automotive Applications	Li Wei Yao	Industrial Technology Research Institute

Note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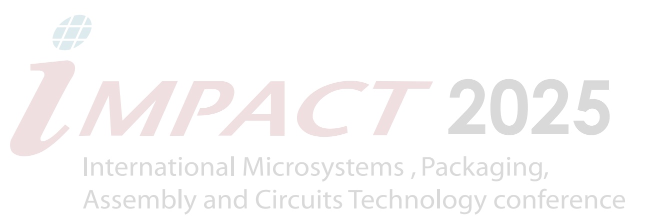

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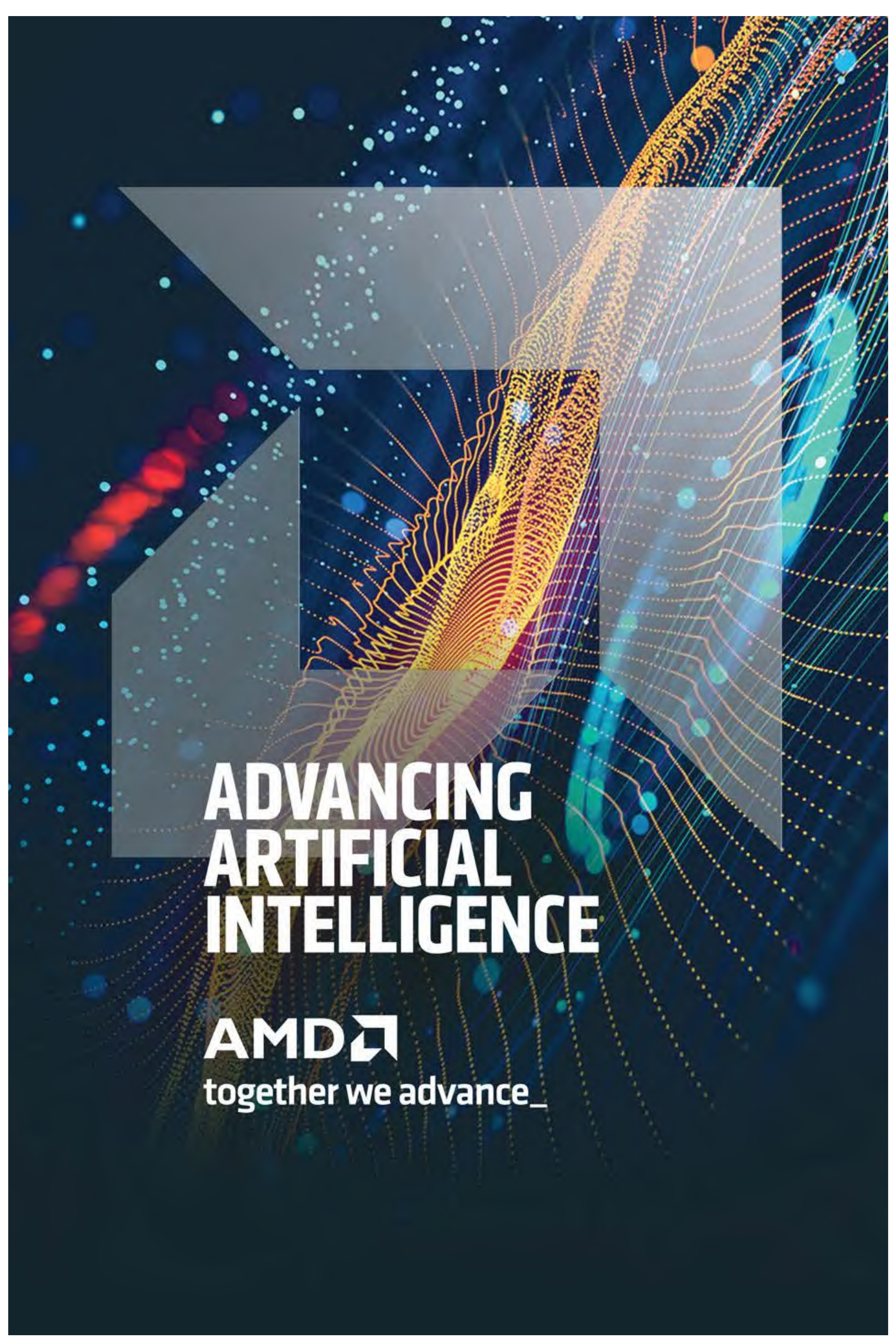
Note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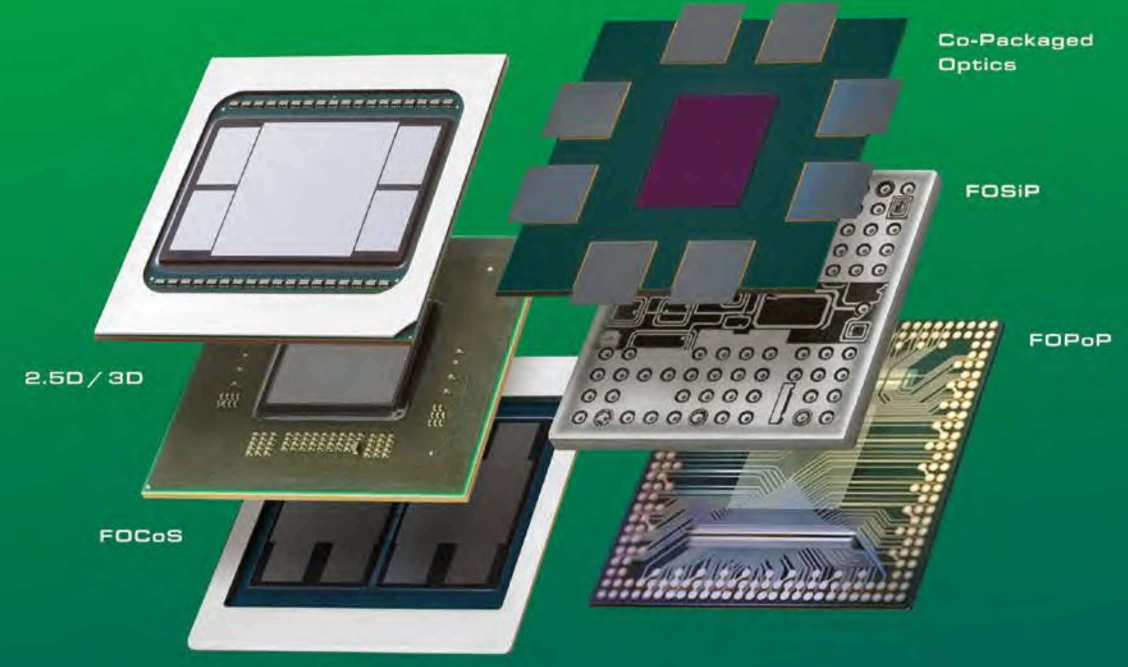

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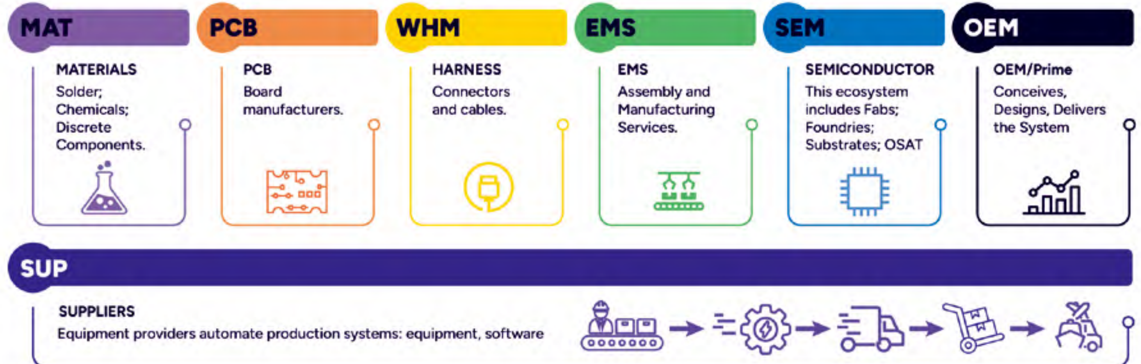

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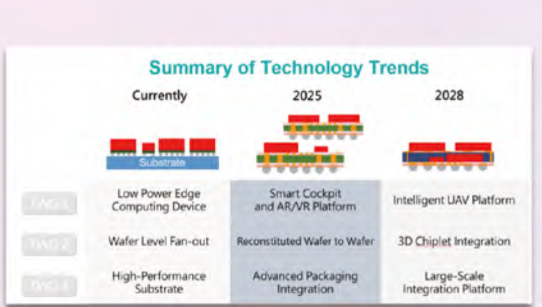
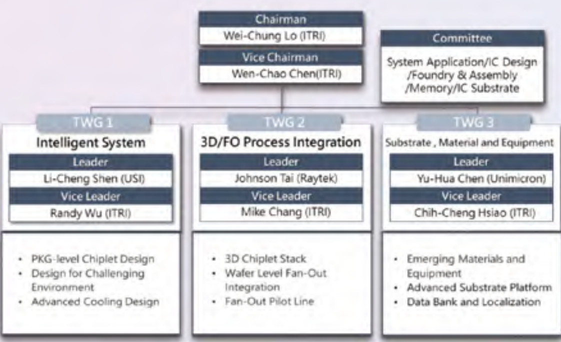
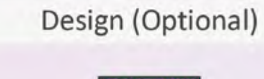
- To complete platform for structure evaluation and proof of concept with ITRI's innovative pilot line
- To verify platform of high-performance & large-scale integration



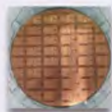


ITRI's Fan-out RDL Shuttle Service Items



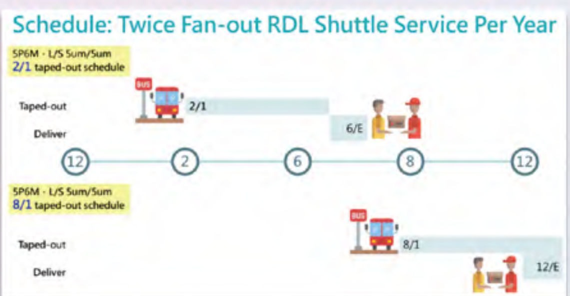
Fan-out RDL Shuttle Service

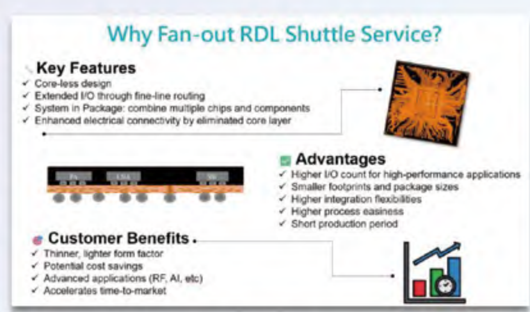
- Package RDL Design
- Multilayer Layout Design
- Simulation & Analysis



- Mask fabrication
- RDL process
- Bumping Process

- Assembly
- Molding
- BGA





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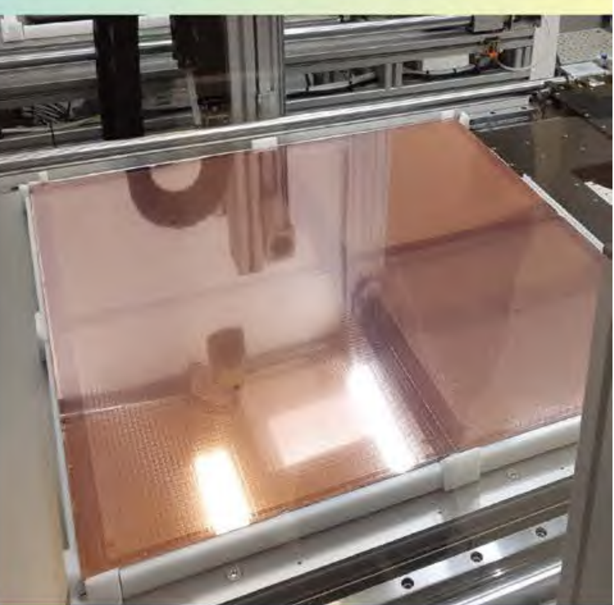
Lam Research Salzburg GmbH

Process solutions for advanced wet chemical panel applications including etching, stripping and electrochemical deposition.



Key Customer Benefits

- Superior processing uniformity
- Extendable platforms to support increasing demand
- Processing of different substrate sizes on one platform
- Worldwide service and support
- Substrate size from 300mm to 650x650mm

SABRE® 3D FP (Flat Panel)

The SABRE® 3D FP is a versatile and modular tool designed for single panel processing. It supports substrates up to 310x310mm and offers multiple processing capabilities. Its advanced features ensure high precision and efficiency in various applications.

Process capability: TGV, RDL, bumps, pads, pillars...

Kallisto Product Family

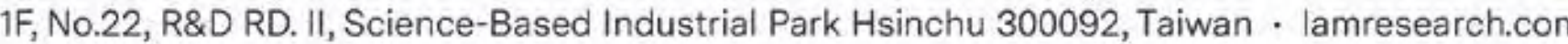
Kallisto enables fine line plating on various materials including organic and glass core technologies. Processing can be single or dual sided depending on the application.

Process capability: TGV, RDL, bumps, pads, pillars...

Phoenix Product Family

Designed with the goal to redefine cost of ownership, Phoenix delivers unique technologies in the panel level packaging industry together with a respectful usage of its operating utilities.

Process capability: TGV, RDL, bumps, pillars, PR-strip, PR-development, clean, metal etch...



mks
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Cupraganth® MV – Redefining electroless copper activation
Cupraganth MV is the world's first Pd-free electroless copper activation solution. It is transforming the manufacture of substrates for advanced packaging. Based on an innovative colloidal copper technology, it supersedes traditional Pd-based methods and delivers both performance and cost benefits. As the Cupraganth MV layer is removed simultaneously with the bulk copper layer, you can simplify your process and achieve finer features by eliminating the need for an additional Pd seed etch. Additionally, take advantage of the stable price of copper to ensure a lower cost of ownership (CoO) with greater financial predictability. Cupraganth MV offers improved yields, and finer track spacing, and works seamlessly with tartrate-based electroless copper baths. The robust and efficient 4-step process assures exceptional coverage and peel strength comparable to ionic Pd technology. Choose Cupraganth MV for superior performance, reduced costs, and breakthrough innovation in package substrate manufacturing.
To find out more about Cupraganth® MV at MKS' Atotech, scan the QR Code to the right.
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www.atotech.com

Qnity 啟諾迪

DuPont Electronics

攜手成就明日科技

Qnity啟諾迪致力於與尖端技術的客戶密切合作，推動人工智慧、先進計算和新一代設備內外部連接技術的革命性進展。從創新的半導體晶片製造解決方案到在複雜電子系統中實現高速傳輸，憑藉高性能材料及其專業整合能力，啟諾迪不斷推進科技邊界，助力未來科技飛躍。

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*The intended separation of Qnity Electronics, Inc., targeted for completion on November 1, 2025, is subject to satisfaction of customary conditions, including final approval by DuPont's Board of Directors, receipt of tax opinion from counsel, the completion and effectiveness of a Form 10 registration statement with the U.S. Securities and Exchange Commission, applicable regulatory approvals and satisfactory completion of financing. More information about the intended separation can be found at https://www.investors.dupont.com.

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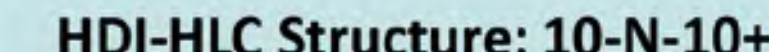
HLC PCB
(High Layer Count PCB)

Technology Roadmap

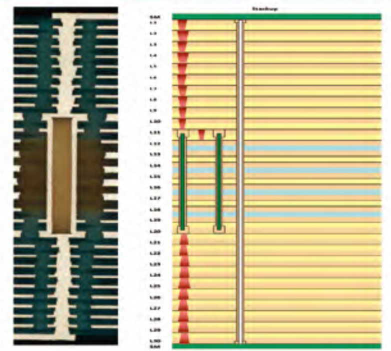
Parameters Feature	2025	2026	2027
Structure (mm)			
Panel Size W x L	610 x 812	610 x 812	610 x 812
Overall Thickness	1.8 ~ 7.2	1.8 ~ 8.0	1.8 ~ 8.0
Layer Count	16~60L	16~66L	16~72L
Line Capability(um)			
Min. Line/Spacing (Inner)	50/50 (*)	40/50 (*)	40/50 (*)
Min. Line/Spacing (Outer)	100/100(**)	75/75(**)	75/75(**)
Through Vias (um)			
PTH Size (Finish)	100	100	100
PTH Size (Drill)	150	150	150
PTH Pad Size (D=Drill)	D+150	D+150	D+150
Max. Aspect Ratio	32:1	36:1	40:1
Tolerance Capability (um)			
Layer to Layer Reg. Tolerance	<75	<75	<50
Solder Mask Reg. Tolerance	<25	<20	<20
Backdrill Stub Length (mil)	4+/-2	4+/-2	2+/-2

Note *: Base on Cu thickness 18~22 (um) ; Note **: Base on Cu thickness 40~50 (um)

Leading Technology

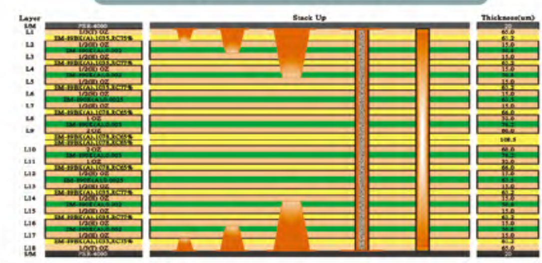


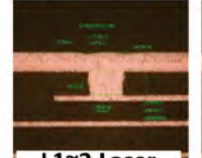
HDI-HLC Structure: 10-N-10+



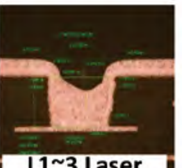
Structure	30L
Stack up	VIPPO + laser via
Number of laminates	11
Thickness (mm)	3.0
Drill size (mm)	0.2
Surface finish	OSP

Skip Via Technology

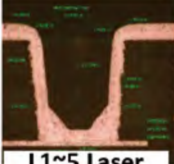




L1~2 Laser



L1~3 Laser



L1~5 Laser

Structure	18L
Stack up	Skip via + laser via
Thickness (mm)	1.57
Surface finish	ENIG

ICEP-HBS 2026

2026 International Conference on Electronics Packaging
and Hybrid Bonding Symposium

Date: April 14 - 18, 2026 "On-site Only"
Venue: International Conference Center Hiroshima, Japan

About ICEP

ICEP is the largest international conference on electronic packaging in Japan, attracting more than 900 attendees and hosting about 35 technical sessions. ICEP provides a strong platform to demonstrate your technologies and products as well as expand your customer network. It is jointly sponsored by JIEP, IEEE EPS, IEEE EPS Japan Chapter, iMAPS, and SMTA. The conference has technical sessions covering a wide range of topics including advanced packaging, design, modeling and reliability, emerging technologies, high-speed, wireless & components, interconnections, materials and processes, optoelectronics, power electronics integration, and thermal management. Since its inauguration in 2001, ICEP has developed into a highly reputed electronics packaging conference in Japan, attended by world-renowned experts in all aspects related to packaging technologies from all over the world.

Contact

Secretariat of ICEP 2026 The Japan Institute of Electronics Packaging (JIEP)
E-mail: icep2026@jiep.or.jp
URL: https://www.jiep.or.jp/icep/

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ISMP 2025
The 23rd International Symposium on Microelectronics and Packaging (ISMP)
November 4Tue~7Fri, 2025
Bareumi Hotel Inter-Burgo Daegu,
Daegu Metropolitan City, Korea
DAEGU
INVITATION
The ISMP organized by KMEPS (The Korean Microelectronics and Packaging Society) presents a valuable chance to share the latest electronic packaging technologies including novel packaging technologies, packaging materials, process, equipment, design, reliability and so on. The ISMP 2025 organizing committee promises to provide an outstanding and fruitful program, which will be a great opportunity that you do not miss.
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CEO
Chipletz, Inc., USA
Ho-Young Son
Vice President
SK hynix Inc., Korea
KEYNOTE SPEAKER
Sung Kyu Lim
Professor
USC (University of Southern California), USA
Dae-Woo Kim
Vice President
Samsung Electronics Co., Ltd., Korea
Choon Heung Lee
Senior Vice President
Intel Corporation, USA
Subramanian S. Iyer
Professor
UCLA (University of California, Los Angeles), USA
Chee Ping Lee
Technical Director
Lam Research Corporation, Singapore
TBD
Samsung Electro-Mechanics Co., Ltd., Korea
SYMPOSIUM TOPICS
1.Design and Simulation 2.Packaging Process 3.Substrate and Interposers 4.Devices and Components
5.Materials Technology 6.Equipment Technology 7.Metrology and Inspections 8.Reliability Engineering

20 LEGACY Explorer Challenge

Mission 1 : Stamp Collect

Complete the check-in mission at designated locations to redeem the exclusive IMPACT 20th Anniversary gift.

Mission 2: Lucky Draw

1. Join the Open Seminar on the 4th floor exhibition hall on Oct. 23 for a chance to win an iPad or AirPods.
2. Present your IMPACT Badge at the designated location on Oct. 24 to claim a special gift (limited).

Event	Date	Time	Location
Stamp Coollect	OCT. 21(TUE)	13:30-17:30	North Elevator @ 5F, TaiNEX 1
	OCT. 22(WED)	10:30-17:30	North Elevator @ 5F, TaiNEX 1
	OCT. 23(THU)	10:30-17:30	North Elevator @ 5F, TaiNEX 1
Lucky Draw		15:00-15:10	Open Seminar(L-1308) @ 4F, TaiNEX 1
	OCT. 24(FRI)	10:00-12:00	Bookstore(N-1431)@4F, TaiNEX 1

iMPACT 2026

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